# 512Kx16 CMOS EEPROM MODULE

## FEATURES

- Access Time of 140, 150, 200ns
- Packaging:
  - 68 lead, 40mm Hermetic CQFP (Package 501)
- Organized as 4 banks of 128Kx16
- Write Endurance 10,000 Cycles
- Data Retention Ten Years Minimum
- Military Temperature Range
- Low Power CMOS

- Automatic Page Write Operation
- Page Write Cycle Time: 10ms Max
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- 8 Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
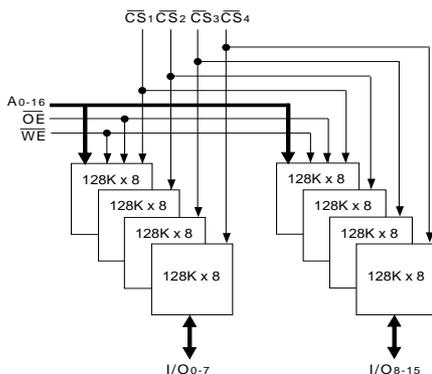- Weight - 20 grams typical

## FIG. 1  PIN CONFIGURATION

### TOP VIEW
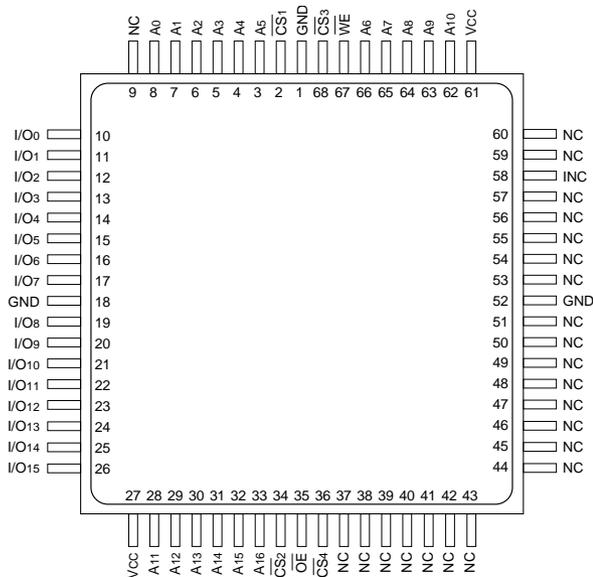


### PIN DESCRIPTION

| Pin | Description |
|-----|-------------|
| I/O$_{0-15}$ | Data Inputs/Outputs |
| A$_{0-16}$ | Address Inputs |
| $\overline{WE}$ | Write Enable |
| $\overline{CS}_{1-4}$ | Chip Selects |
| $\overline{OE}$ | Output Enable |
| V$_{CC}$ | Power Supply |
| GND | Ground |
| NC | Not Connected |

### BLOCK DIAGRAM



**NOTE:**

$\overline{CS}_{1-4}$ are used as bank selects. During reads, only one $\overline{CS}$x can be active at one time.
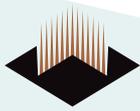
## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | | Unit |
|---|---|---|---|
| Operating Temperature | $T_A$ | -55 to +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |
| Signal Voltage Relative to GND | $V_G$ | -0.6 to +6.25 | V |
| Voltage on $\overline{OE}$ and A9 | | -0.6 to +13.5 | V |

**NOTE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | $V_{CC}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | +0.8 | V |
| Operating Temp. (Mil.) | $T_A$ | -55 | +125 | °C |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | Data I/O |
|---|---|---|---|---|
| H | X | X | Standby | High Z |
| L | L | H | Read | Data Out |
| L | H | L | Write | Data In |
| X | H | X | Out Disable | High Z/Data Out |
| X | X | H | Write | |
| X | L | X | Inhibit | |

## CAPACITANCE
($T_A$ = +25°C)

| Parameter | Symbol | Conditions | Max | Unit |
|---|---|---|---|---|
| $\overline{OE}$ capacitance | $C_{OE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 50 | pF |
| $\overline{WE}$ capacitance | $C_{WE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 50 | pF |
| $CS_{1-4}$ capacitance | $C_{CS}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 25 | pF |
| Data I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V, f = 1.0 MHz | 40 | pF |
| Address input capacitance | $C_{AD}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 70 | pF |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS
($V_{CC}$ = 5.0V, GND = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | | 10 | µA |
| Operating Supply Current (x16) | $I_{CCx16}$ | $\overline{CS}_1$ = $V_{IL}$, $\overline{OE}$ = $\overline{CS}_{2-4}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 160 | mA |
| Chip Erase Current | $I_{CC1}$ | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 250 | mA |
| Standby Current (CMOS) | $I_{SB}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 5 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2.1mA, $V_{CC}$ = 4.5V | | 0.45 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -400µA, $V_{CC}$ = 4.5V | 2.4 | | V |

NOTE: DC test conditions: $V_{IH}$ = $V_{CC}$ -0.3V, $V_{IL}$ = 0.3V

## FIG. 2
## AC TEST CIRCUIT
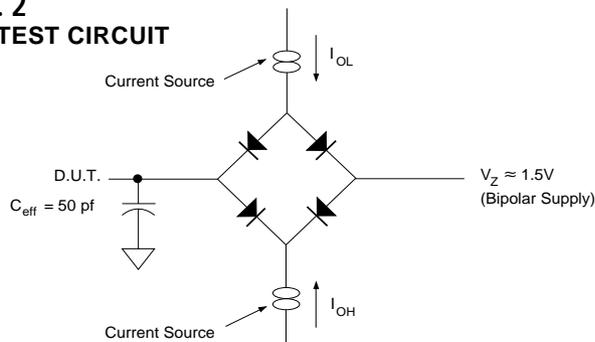


## AC TEST CONDITIONS

| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL}$ = 0, $V_{IH}$ = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

**NOTES:**
$V_Z$ is programmable from -2V to +7V.
$I_{OL}$ & $I_{OH}$ programmable from 0 to 16mA.
Tester Impedance $Z_0$ = 75 Ω.
$V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ & $I_{OH}$ are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

# WRITE

A write cycle is initiated when $\overline{OE}$ is high and a low pulse is on $\overline{WE}$ or $\overline{CS}$ with $\overline{CS}$ or $\overline{WE}$ low. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$ whichever occurs last. The data is latched by the rising edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs first. A word write operation will automatically continue to completion.

## WRITE CYCLE TIMING

Figures 3 and 4 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{CS}$ line low. Write enable consists of setting the $\overline{WE}$ line low. The write cycle begins when the last of either $\overline{CS}$ or $\overline{WE}$ goes low.

The $\overline{WE}$ line transition from high to low also initiates an internal 150 μsec delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the 150 μsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

## AC WRITE CHARACTERISTICS
($V_{CC}$ = 5.0V, GND = 0V, $T_A$ = -55°C to +125°C)

| Write Cycle Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Write Cycle Time, TYP = 6ms | $t_{WC}$ | | 10 | ms |
| Address Set-up Time | $t_{AS}$ | 10 | | ns |
| Write Pulse Width ($\overline{WE}$ or $\overline{CS}$) | $t_{WP}$ | 120 | | ns |
| Chip Select Set-up Time | $t_{CS}$ | 0 | | ns |
| Address Hold Time | $t_{AH}$ | 100 | | ns |
| Data Hold Time | $t_{DH}$ | 10 | | ns |
| Chip Select Hold Time | $t_{CSH}$ | 0 | | ns |
| Data Set-up Time | $t_{DS}$ | 100 | | ns |
| Output Enable Set-up Time | $t_{OES}$ | 10 | | ns |
| Output Enable Hold Time | $t_{OEH}$ | 10 | | ns |
| Write Pulse Width High | $t_{WPH}$ | 50 | | ns |
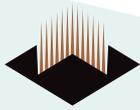
**FIG. 3**
**WRITE WAVEFORM**
**WE CONTROLLED**
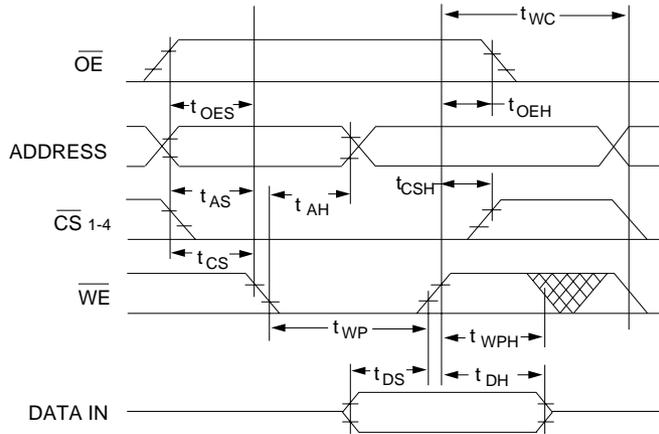


**FIG. 4**
**WRITE WAVEFORM**
**CS CONTROLLED**
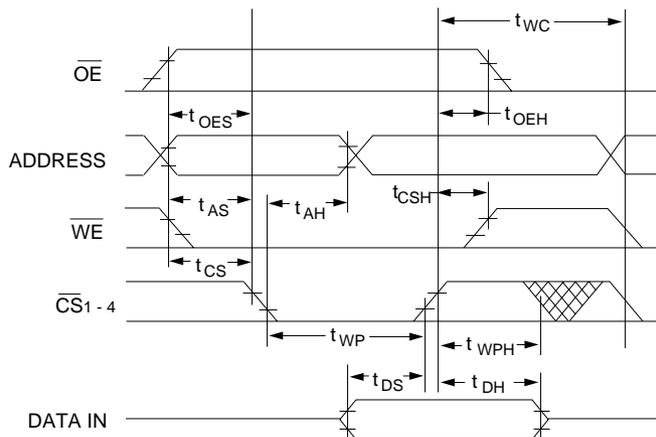
## READ

The module stores data at the memory location determined by the address pins. When $\overline{CS}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, this data is present on the outputs. When $\overline{CS}$ and $\overline{OE}$ are high, the outputs are in a high impedance state. This two line control prevents bus contention.

### AC READ CHARACTERISTICS
($V_{CC}$ = 5.0V, GND = 0V, $T_A$ = -55°C to +125°C)

| Read Cycle Parameter | Symbol | -140 | | -150 | | -200 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 140 | | 150 | | 200 | | ns |
| Address Access Time | $t_{ACC}$ | | 140 | | 150 | | 200 | ns |
| Chip Select Access Time | $t_{ACS}$ | | 140 | | 150 | | 200 | ns |
| Output Hold from Add. Change, $\overline{OE}$ or $\overline{CS}$ | $t_{OH}$ | 0 | | 0 | | 0 | | ns |
| Output Enable to Output Valid | $t_{OE}$ | 0 | 50 | 0 | 55 | 0 | 55 | ns |
| Chip Select or $\overline{OE}$ to High Z Output | $t_{DF}$ | | 50 | | 70 | | 70 | ns |

## FIG. 5
### READ WAVEFORM
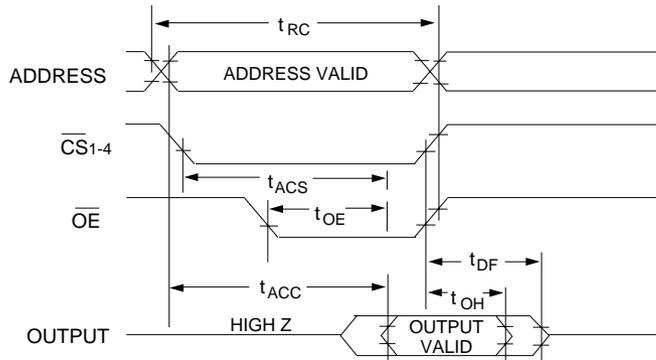


**NOTES:**
$\overline{OE}$ may be delayed up to $t_{ACS}$ - $t_{OE}$ after the falling edge of $\overline{CS}$ without impact on $t_{OE}$ or by $t_{ACC}$ - $t_{OE}$ after an address change without impact on $t_{ACC}$.
$\overline{CS}_{1-4}$ are used as bank selects.
During reads, only one $\overline{CS}_x$ can be active at one time.
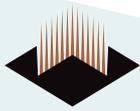
## DATA POLLING

The module offers a data polling feature which allows a faster method of writing to the device. Figure 6 shows the timing diagram for this function. During a word or page write cycle, an attempted read of the last word written will result in the complement of the written data on $I/O_7$ and $I/O_{15}$. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

### DATA POLLING CHARACTERISTICS
($V_{CC}$ = 5.0V, GND = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Data Hold Time | $t_{DH}$ | 10 | | ns |
| $\overline{OE}$ Hold Time | $t_{OEH}$ | 10 | | ns |
| $\overline{OE}$ To Output Valid | $t_{OE}$ | | 55 | ns |
| Write Recovery Time | $t_{WR}$ | 0 | | ns |

## FIG. 6
### DATA POLLING WAVEFORM
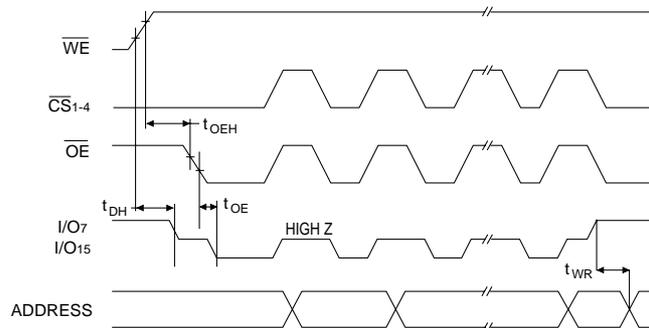
## PAGE WRITE OPERATION

The module has a page write operation that allows one to 128 words of data to be written into the device and consecutively loads during the internal programming period. Successive words may be loaded in the same manner after the first data word has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150μs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from $A_0$ through $A_6$ at each write cycle. In this manner a page of up to 128 words can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150μs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of words will be written at the same time. The internal programming cycle is the same regardless of the number of words accessed.

## PAGE WRITE CHARACTERISTICS

($V_{CC}$ = 5.0V, GND = 0V, $T_A$ = -55°C to +125°C)

| Page Mode Write Characteristics | Symbol | | | Unit |
|---|---|---|---|---|
| Parameter | | Min | Max | |
| Write Cycle Time, TYP = 6ms | $t_{WC}$ | | 10 | ms |
| Address Set-up Time | $t_{AS}$ | 0 | | ns |
| Address Hold Time (1) | $t_{AH}$ | 50 | | ns |
| Data Set-up Time | $t_{DS}$ | 50 | | ns |
| Data Hold Time | $t_{DH}$ | 0 | | ns |
| Write Pulse Width | $t_{WP}$ | 100 | | ns |
| Word Load Cycle Time | $t_{BLC}$ | | 150 | μs |
| Write Pulse Width High | $t_{WPH}$ | 50 | | ns |

1. Page address must remain valid for duration of write cycle.

### FIG. 7
### PAGE MODE
### WRITE WAVEFORM
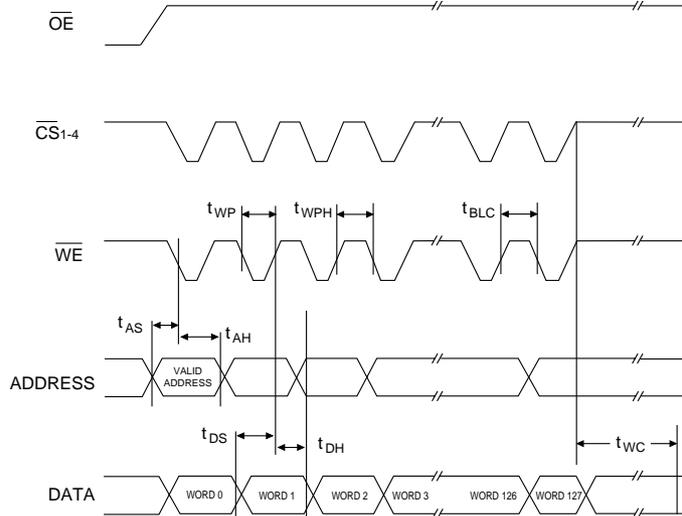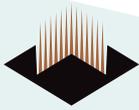
**FIG. 8**
**SOFTWARE DATA PROTECTION**
**ENABLE ALGORITHM[1]**
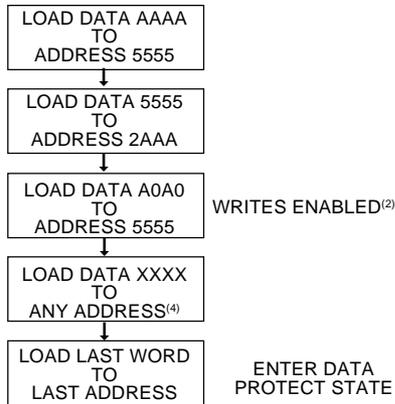


LOAD DATA AAAA TO ADDRESS 5555

LOAD DATA 5555 TO ADDRESS 2AAA

LOAD DATA A0A0 TO ADDRESS 5555 — WRITES ENABLED[2]

LOAD DATA XXXX TO ANY ADDRESS[4]

LOAD LAST WORD TO LAST ADDRESS — ENTER DATA PROTECT STATE

**NOTES:**
1. Data Format: $I/O_{15-0}$ (Hex); Address Format: $A_{16-0}$ (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 words of data may be loaded.

## FIG. 9
## SOFTWARE DATA PROTECTION
## DISABLE ALGORITHM[1]

```
                    ┌─────────────────────┐
                    │   LOAD DATA AAAA     │
                    │         TO           │
                    │   ADDRESS 5555       │
                    └─────────┬───────────┘
                              ▼
                    ┌─────────────────────┐
                    │   LOAD DATA 5555     │
                    │         TO           │
                    │   ADDRESS 2AAA       │
                    └─────────┬───────────┘
                              ▼
                    ┌─────────────────────┐
                    │   LOAD DATA 8080     │
                    │         TO           │
                    │   ADDRESS 5555       │
                    └─────────┬───────────┘
                              ▼
                    ┌─────────────────────┐
                    │   LOAD DATA AAAA     │
                    │         TO           │
                    │   ADDRESS 5555       │
                    └─────────┬───────────┘
                              ▼
                    ┌─────────────────────┐
                    │   LOAD DATA 5555     │
                    │         TO           │
                    │   ADDRESS 2AAA       │
                    └─────────┬───────────┘
                              ▼
                    ┌─────────────────────┐
                    │   LOAD DATA 2020     │
                    │         TO           │
                    │   ADDRESS 5555       │
   EXIT DATA [3]    └─────────┬───────────┘
   PROTECT STATE              ▼
                    ┌─────────────────────┐
                    │   LOAD DATA XXXX     │
                    │         TO           │
                    │   ANY ADDRESS[4]     │
                    └─────────┬───────────┘
                              ▼
                    ┌─────────────────────┐
                    │   LOAD LAST WORD     │
                    │         TO           │
                    │   LAST ADDRESS       │
                    └─────────────────────┘
```

**NOTES:**
1. Data Format: $I/O_{15-0}$ (Hex);
   Address Format: $A_{16-0}$ (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
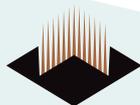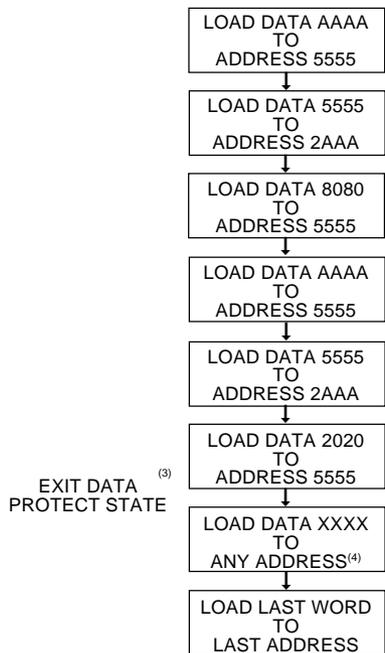4. 1 to 128 words of data may be loaded.

## SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the module has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code words to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three-word write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-word command sequence will start the internal write timers. No data will be written to the device, however, for the duration of $t_{WC}$. The write protection feature can be disabled by a six-word write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K-word block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

## HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the module. These are included to improve reliability during normal operation:

a) **$V_{CC}$ power on delay**
As $V_{CC}$ climbs past 3.8V typical the device will wait 5 msec typical before allowing write cycles.

b) **$V_{CC}$ sense**
While below 3.8V typical write cycles are inhibited.

c) **Write inhibiting**
Holding $\overline{OE}$ low and either $\overline{CS}$ or $\overline{WE}$ high inhibits write cycles.

d) **Noise filter**
Pulses of <8ns (typ) on $\overline{WE}$ or $\overline{CS}$ will not initiate a write cycle.

## PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

## ORDERING INFORMATION

W E 512K16 - XXX G4 X X

**LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

**PROCESSING:**

Q = MIL-STD-883 Compliant

M = Military Screened    -55°C to +125°C

I = Industrial    -40°C to +85°C

C = Commercial    0°C to +70°C

**PACKAGE:**

G4 = 40mm Ceramic Quad Flat Pack, CQFP (Package 501)

**ACCESS TIME (ns)**

**ORGANIZATION, 4 banks of 128Kx16**

**EEPROM**

**WHITE ELECTRONIC DESIGNS CORP.**