8Mx72 Synchronous DRAM + 8Mb Flash Mixed Module Multi-Chip Package *ADVANCED**

FEATURES

- Package:
  - 275 Plastic Ball Grid Array (PBGA), 32mm x 25mm
- Commercial, Industrial and Military Temperature Ranges
- Weight:
  - WEDPNF8M721V-XBX - 2.5 grams typical

SDRAM PERFORMANCE FEATURES

- Organized as 8M x 72
- High Frequency = 100, 125MHz
- Single 3.3V ±0.3V power supply
- Fully Synchronous; all signals registered on positive edge of system clock cycle
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable Burst length 1,2,4,8 or full page
- 4096 refresh cycles

FLASH PERFORMANCE FEATURES

- User Configurable as 1Mx8 or 512Kx16
- Access Times of 100, 120, 150ns
- 3.3 Volt for Read and Write Operations
- 1,000,000 Erase/Program Cycles
- Sector Architecture
  - One 16KByte, two 8KBytes, one 32KByte, and fif teen 64KBytes in byte mode
  - One 8K word, two 4K words, one 16K word, and fifteen 32K word sectors in word mode.
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Boot Code Sector Architecture (Bottom)
- Embedded Erase and Program Algorithms
- Erase Suspend/Resume
  - Supports reading data from or programing data to a sector not being erased

BENEFITS

- 42% SPACE SAVINGS
- Reduced part count
- Reduced I/O count
  - 14% I/O Reduction
- Suitable for hi-reliability applications
- SDRAM Upgradeable to 16M x 72 density (contact factory for information)
- Flash upgradeable to 2M x 8 (or 1M x 16 or 512K x 32) density

** This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

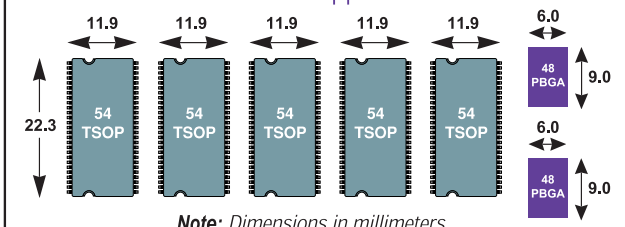
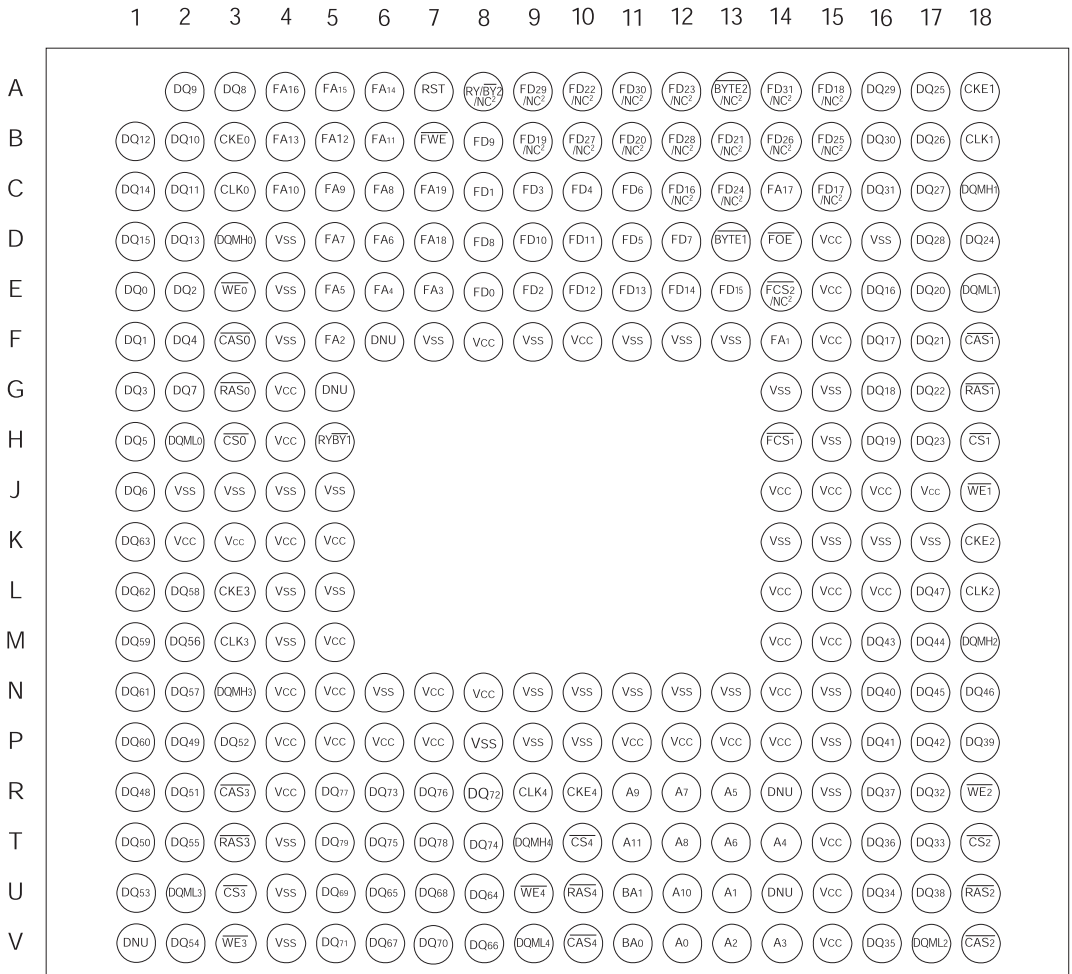
	Discrete Approach	ACTUAL SIZE	SAVINGS
	 **Note:** *Dimensions in millimeters*		
Area	5 x 265mm² + 2 x 54mm² = 1433mm²	800mm²	44%
I/O Count	5 x 54 pins + 2 x 48 balls = 366 connections	275 balls	25%

FIG. 1 PIN CONFIGURATION

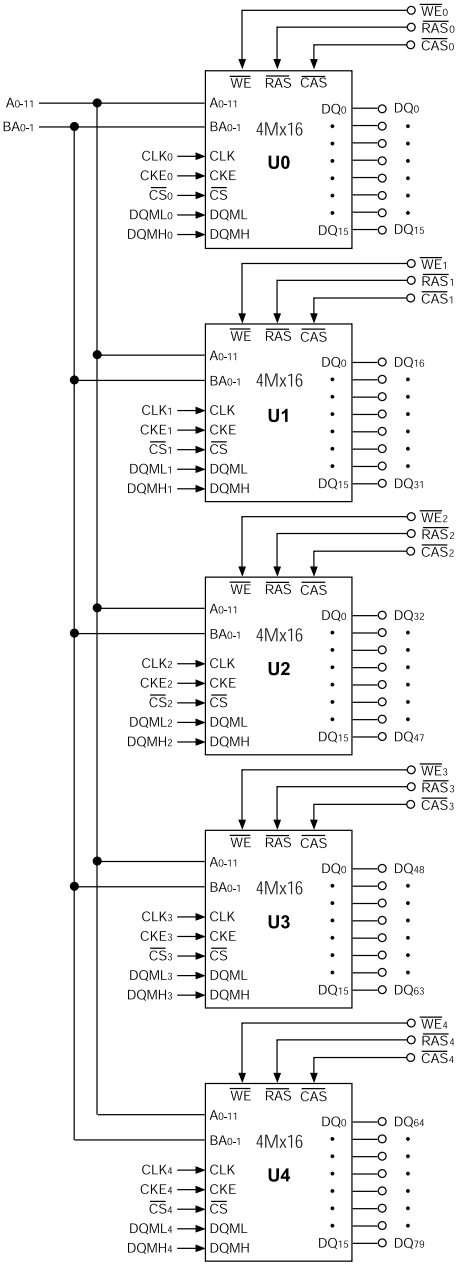
TOP VIEW



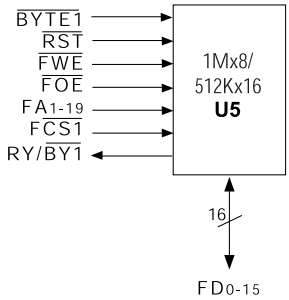
NOTES:
1. DNU = Do Not Use
2. FD16-31, BYTE2, RY/BY2 are NC in this part, and used for flash upgraded to WEDPN8M722V-XBX (2x8M Flash).

FIG. 2 FUNCTIONAL BLOCK DIAGRAMS

SDRAM



FLASH



PACKAGE PINOUT LISTING

Signal Name	Pin Number
Vcc	D15, E15, F8, F10, F15, G4, H4, J14, J15, J16, J17, K2, K3, K4, K5, L14, L15, L16, M5, M14, M15, N4, N5, N7, N8, N14, P4, P5, P6, P7, P11, P12, P13, P14, R4, T15, U15, V15
GND	D4, D16, E4, F4, F7, F9, F11, F12, F13, G14, G15, H15, J2, J3, J4, J5, K14, K15, K16, K17, L4, L5, M4, N6, N9, N10, N11, N12, N13, N15, P8, P9, P10, P15, R15, T4, U4, V4
FD0 - 15	E8, C8, E9, C9, C10, D11, C11, D12, D8, B8, D9, D10, E10, E11, E12, E13
RY$\overline{BY}$1	H5
$\overline{RST}$	A7
BYTE1	D13
FD16* - 31*	C12, C15, A15, B9, B11, B13, A10, A12, C13, B15, B14, B10, B12, A9, A11, A14
RY$\overline{BY}$2*	A8
$\overline{BYTE2}$*	A13
FA1-19	F14, F5, E7, E6, E5, D6, D5, C6, C5, C4, B6, B5, B4, A6, A5, A4, C14, D7, C7
$\overline{FCS1}$	H14
$\overline{FCS2}$*	E14
$\overline{FWE}$	B7
$\overline{FOE}$	D14
A0 - A11	V12, U13, V13, V14, T14, R13, T13, R12, T12, R11, U12, T11
BA0 - 1	U11, V11
$\overline{CS0}$	H3
$\overline{WE0}$	E3
$\overline{CLK0}$	C3
CKE0	B3
$\overline{RAS0}$	G3
$\overline{CAS0}$	F3
DQML0	H2
DQMH0	D3
$\overline{CS1}$	H18
$\overline{WE1}$	J18
CLK1	B18
CKE1	A18
$\overline{RAS1}$	G18
$\overline{CAS1}$	F18
DQML1	E18
DQMH1	C18
$\overline{CS2}$	T18
$\overline{WE2}$	R18
CLK2	L18
CKE2	K18
$\overline{RAS2}$	U18
$\overline{CAS2}$	V18
DQML2	V17
DQMH2	M18
$\overline{CS3}$	U3
$\overline{WE3}$	V3
CLK3	M3
CKE3	L3
$\overline{RAS3}$	T3

**FD16-31, RY/$\overline{BY}$2, $\overline{BYTE2}$ are NC in this part, and used for flash upgrade to WEDPNF8M722V-XBX*

PACKAGE PINOUT LISTING (CONTINUED)

Signal Name	Pin Number
$\overline{CAS3}$	R3
DQML3	U2
DQMH3	N3
$\overline{CS4}$	T10
$\overline{WE4}$	U9
CLK4	R9
CKE4	R10
$\overline{RAS4}$	U10
$\overline{CAS4}$	V10
DQML4	V9
DQMH4	T9
DQ0 - 15	E1, F1, E2, G1, F2, H1, J1, G2, A3, A2, B2, C2, B1, D2, C1, D1,
DQ16 - 31	E16, F16, G16, H16, E17, F17, G17, H17, D18, A17, B17, C17, D17, A16, B16, C16
DQ32 - 47	R17, T17, U16, V16, T16, R16, U17, P18, N16, P16, P17, M16, M17, N17, N18, L17
DQ48 - 63	R1, P2, T1, R2, P3, U1, V2, T2, M2, N2, L2, M1, P1, N1, L1, K1
DQ64 - 79	U8, U6, V5, V6, U7, U5, V7, V8, R8, R6, T8, T6, R7, R5, T7, T5
DNU	F6, G5, R14, U14, V1

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to Vcc +0.5	V
Operating Temperature T_A (Mil)	-55 to +125	°C
Operating Temperature T_A (Ind)	-40 to +85	°C
Storage Temperature, Plastic	-65 to +150	°C
Flash Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

SDRAM CAPACITANCE (NOTE 2)

Parameter	Symbol	Max	Unit
Input Capacitance: CLK	C_{I1}	10	pF
Addresses, BA_{0-1} Input Capacitance	C_A	35	pF
Input Capacitance: All other input-only pins	C_{I2}	10	pF
Input/Output Capacitance: I/Os	C_{IO}	12	pF

FLASH DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (NOTES 1, 3)
(VCC = +3.3V ±0.3V; TA = -55°C TO +125°C)

Parameter/Condition	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	3	3.6	V
Input High Voltage: Logic 1; All inputs (4)	V_{IH}	0.7 x Vcc	V_{CC} + 0.3	V
Input Low Voltage: Logic 0; All inputs (4)	V_{IL}	-0.3	0.8	V
SDRAM Input Leakage Current: Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-5	5	µA
SDRAM Input Leakage Address Current (All other pins not under test = 0V)	I_I	-25	25	µA
SDRAM Output Leakage Current: I/Os are disabled; 0V ≤ V_{OUT} ≤ V_{CC}	I_{OZ}	-5	5	µA
SDRAM Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V
SDRAM Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V
Flash Flash Input Leakage Current (V_{CC} = 3.6, V_{IN} = GND or V_{CC})	I_{LI}		10	µA
Flash Output Leakage Current (V_{CC} = 3.6, V_{IN} = GND or V_{CC})	I_{LOx8}		10	µA
Flash Output High Voltage (I_{OH} = -2.0 mA, V_{CC} = 3.0)	V_{OH1}	0.85 x V_{CC}		V
Flash Output Low Voltage (I_{OL} = 5.8 mA, V_{CC} = 3.0)	V_{OL}		0.45	V
Flash Low V_{CC} Lock-Out Voltage (5)	V_{LKO}	2.3	2.5	V

NOTES:
1. All voltages referenced to VSS.
2. This parameter is not tested but guaranteed by design. f = 1 MHz, TA = 25°C.
3. An initial pause of 100ms is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VCC must be powered up simultaneously.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
4. VIH overshoot: VIH (MAX) = VCC + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot: VIL (MIN) = -2V for a pulse width ≤ 3ns.
5. Guaranteed by design, but not tested.

ICC SPECIFICATIONS AND CONDITIONS (NOTES 1,2,3,4)
(VCC = +3.3V ±0.3V; TA = -55°C TO +125°C)

Parameter/Condition	Symbol	Max	Units
SDRAM Operating Current: Active Mode; Burst = 2; Read or Write; tRC = tRC (min); CAS latency = 3 (5, 6, 7); $\overline{FCS}$ = High	ICC1	750	mA
SDRAM Standby Current: Active Mode; CKE = HIGH; $\overline{CS}$ = HIGH; $\overline{FCS}$ = High; All banks active after tRCD met; No accesses in progress (5, 7, 8)	ICC3	250	mA
SDRAM Operating Current: Burst Mode; Continuous burst; $\overline{FCS}$ = High Read or Write; All banks active; CAS latency = 3 (5, 6, 7)	ICC4	750	mA
SDRAM Self Refresh Current; $\overline{FCS}$ = High (14)	ICC7	10	mA
Flash VCC Active Current for Read : $\overline{FCS}$ = VIL, $\overline{FOE}$ = VIH, f = 5MHz (9), $\overline{CS}$ = High, CKE = Low	IFCC1	32	mA
Flash VCC Active Current for Program or Erase: $\overline{FCS}$ = VIL, $\overline{FOE}$ = VIH, $\overline{CS}$ = High, CKE = Low	IFCC2	50	mA
Standby Current: VCC = 3.6 Max, $\overline{FCS}$ = VIH, $\overline{CS}$ = High, $\overline{CKE}$ = Low	ICC3	20	mA

NOTES:
1. All voltages referenced to VSS.
2. An initial pause of 100ms is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VCC must be powered up simultaneously.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
3. AC timing and ICC tests have VIL = 0V and VIH = 3V, with timing referenced to 1.5V crossover point.
4. ICC specifications are tested after the device is properly initialized.
5. ICC is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. The ICC current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
7. Address transitions average one transition every two clocks.
8. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
9. The ICC current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with OE at VIH.
10. ICC active while Embedded Algorithm (program or erase) is in progress.
11. Maximum ICC specifications are tested with VCC = VCC Max.
12. Automatic sleep mode enables the low power mode when addressed remain stable for tacc + 30 ns.
13. SDRAM inactive and in Power Down mode, all banks idle.
14. Self refresh available in commercial and industrial temperatures only.

SDRAM DESCRIPTION

The 64MByte (512Mb) SDRAM is a high-speed CMOS, dynamic random-access ,memory using 5 chips containing 134, 217, 728 bits. Each chip is internally configured as a quad-bank DRAM with a synchronous interface. Each of the chip's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64MB SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 64MB SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode.

All inputs and outputs are LVTTL compatible. SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

SDRAM FUNCTIONAL DESCRIPTION

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-11 select the row). The address bits (A0-8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

INITIALIZATION

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to VDD and VDDQ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or a NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register programming. Because the Mode Register will power up in an unknown state, it should be loaded prior to applying any operational command.

REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 3. The Mode Register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10 and M11 are reserved for future use.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

BURST LENGTH

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 3. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-8 when the burst length is set to two; by A2-8 when the burst length is set to four; and by A3-8 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

CAS LATENCY

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge

FIG. 3 MODE REGISTER DEFINITION

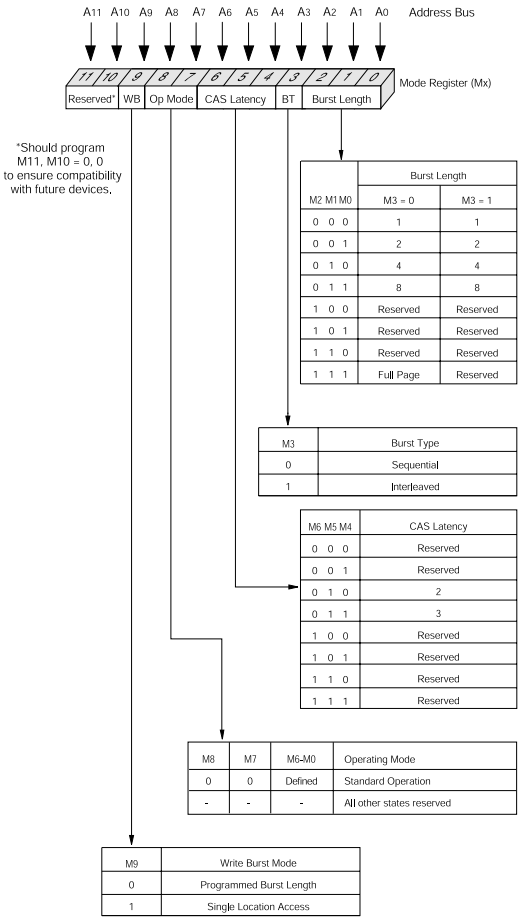


TABLE 1 - BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-9/8/7 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... …Cn - 1, Cn…	Not Supported

NOTES:

1. For full-page accesses: y = 512.

2. For a burst length of two, A1-8 select the block-of-two burst; A0 selects the starting column within the block.

3. For a burst length of four, A2-8 select the block-of-four burst; A0-1 select the starting column within the block.

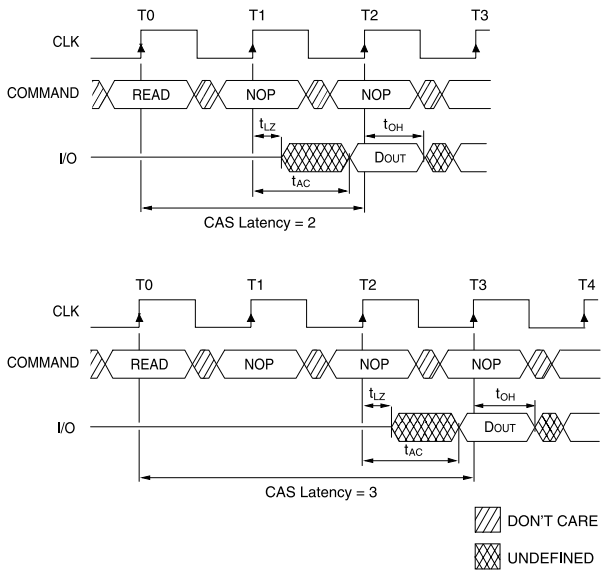
4. For a burst length of eight, A3-8 select the block-of-eight burst; A0-2 select the starting column within the block.

5. For a full-page burst, the full row is selected and A0-8 select the starting column.

6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

7. For a burst length of one, A0-8 select the unique column to be accessed, and Mode Register bit M3 is ignored.

FIG. 4 CAS LATENCY



n+m. The I/Os will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the I/Os will start driving after T1 and the data will be valid by T2. Table 2 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

OPERATING MODE

The normal operating mode is selected by setting M7and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

WRITE BURST MODE

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

COMMANDS

The Truth Table provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TABLE 2 - CAS LATENCY

SPEED	ALLOWABLE OPERATING FREQUENCY (MHZ)	
	CAS LATENCY = 2	CAS LATENCY = 3
-100	≤ 75	≤ 100
-125	≤ 100	≤ 125

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS is $\overline{\text{LOW}}$). This pre-

TABLE 3 TRUTH TABLE - COMMANDS AND DQM OPERATION (NOTE 1)

NAME (FUNCTION)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	I/Os
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X
NO OPERATION (NOP)	L	H	H	H	X	X	X
ACTIVE (Select bank and activate row) (3)	L	L	H	H	X	Bank/Row	X
READ (Select bank and column, and start READ burst) (4)	L	H	L	H	L/H [8]	Bank/Col	X
WRITE (Select bank and column, and start WRITE burst) (4)	L	H	L	L	L/H [8]	Bank/Col	Valid
BURST TERMINATE	L	H	H	L	X	X	Active
PRECHARGE (Deactivate row in bank or banks) (5)	L	L	H	L	X	Code	X
AUTO REFRESH or SELF REFRESH (Enter self refresh mode) (6, 7)	L	L	L	H	X	X	X
LOAD MODE REGISTER (2)	L	L	L	L	X	Op-Code	X
Write Enable/Output Enable (8)	–	–	–	–	L	–	Active
Write Inhibit/Output High-Z (8)	–	–	–	–	H	–	High-Z

NOTES:

1. CKE is HIGH for all commands shown except SELF REFRESH.

2. A0-11 define the op-code written to the Mode Register.

3. A0-11 provide row address, and BA0, BA1 determine which bank is made active.

4. A0-8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.

5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."

6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.

7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.

8. Activates or deactivates the I/Os during WRITEs (zero-clock delay) and READs (two-clock delay).

vents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The Mode Register is loaded via inputs A0-11. See Mode Register heading in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-8 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the READ burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Read data appears on the I/Os subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding I/Os will be High-Z two clocks later; if the DQM signal was registered LOW, the I/Os will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-8 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the I/Os is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where AUTO PRECHARGE does not apply. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analagous to $\overline{\text{CAS}}$-BEFORE-RAS (CBR) $\overline{\text{REFRESH}}$ in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. Each 128Mb SDRAM requires 4,096 AUTO REFRESH cycles every refresh period (tREF). Providing a distributed AUTO REFRESH command will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRC), once every refresh period (tREF).

SELF REFRESH*

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care," with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to tRAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for tXSR, because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

**Self refresh available in commercial and industrial temperatures only.*

FLASH DESCRIPTION

The 8Mbit 3.3 volt-only Flash memory is organized as 1,048,576 bytes. The byte-wide (x8) data appears on FD0-7; the word-wide (x16) data appears on FD0-15. This device requires only a single 3.3 volt Vcc supply to perform read, program, and erase operations. A standard EPROM programmer can also be used to program and erase the device.

This device features unlock bypass programming and in-system sector protection/unprotection.

This device offers access times of 100, 120 and 150ns, allowing operation without wait states. To eliminate bus contention the device has separate chip select ($\overline{\text{FCS}}$), wite enable ($\overline{\text{FWE}}$) and output enable ($\overline{\text{FOE}}$) controls.

The device requires only a single 3.3 volt power supply for

SDRAM ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CHARACTERISTICS

(NOTES 1, 2, 3, 4, 5)

Parameter		Symbol	-100 Min	-100 Max	-125 Min	-125 Max	Unit
Access time from CLK (pos. edge)	CL = 3	t_{AC}		7		6	ns
	CL = 2	t_{AC}		7		6	ns
Address hold time		t_{AH}	1		1		ns
Address setup time		t_{AS}	2		2		ns
CLK high-level width		t_{CH}	3		3		ns
CLK low-level width		t_{CL}	3		3		ns
Clock cycle time (6)	CL = 3	t_{CK}	10		8		ns
	CL = 2	t_{CK}	13		10		ns
CKE hold time		t_{CKH}	1		1		ns
CKE setup time		t_{CKS}	2		2		ns
$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM hold time		t_{CMH}	1		1		ns
$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM setup time		t_{CMS}	2		2		ns
Data-in hold time		t_{DH}	1		1		ns
Data-in setup time		t_{DS}	2		2		ns
Data-out high-impedance time	CL = 3 (7)	t_{HZ}		7		6	ns
	CL = 2 (7)	t_{HZ}		7		6	ns
Data-out low-impedance time		t_{LZ}	1		1		ns
Data-out hold time (load)		t_{OH}	3		3		ns
Data-out hold time (no load) (8)		t_{OH_N}	1.8		1.8		ns
ACTIVE to PRECHARGE command		t_{RAS}	50	120,000	45	120,000	ns
ACTIVE to ACTIVE command period		t_{RC}	70		68		ns
ACTIVE to READ or WRITE delay		t_{RCD}	20		20		ns
Refresh period (4,096 rows) – Commercial, Industrial		t_{REF}		64		64	ms
Refresh period (4,096 rows) – Military		t_{REF}		16		16	ms
AUTO REFRESH period		t_{RFC}	70		70		ns
PRECHARGE command period		t_{RP}	20		20		ns
ACTIVE bank A to ACTIVE bank B command		t_{RRD}	15		16		ns
Transition time (9)		t_T	0.3	1.2	0.3	1.2	ns
WRITE recovery time	(10)	t_{WR}	1 CLK + 7ns		1 CLK + 7ns		—
	(11)		15		15		ns
Exit SELF REFRESH to ACTIVE command		t_{XSR}	80		78		ns

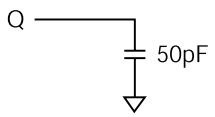
NOTES:

1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.

2. An initial pause of 100ms is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VCC must be powered up simultaneously.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.

3. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.

4. Outputs measured at 1.5V with equivalent load:



5. AC timing and ICC tests have VIL = 0V and VIH = 3V, with timing referenced to 1.5V crossover point.

6. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.

7. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet tOH before going High-Z.

8. Guaranteed by design, but not tested.

9. AC characteristics assume tT = 1ns.

10. Auto precharge mode only. The precharge timing budget (tRP) begins 7.5ns/ 7ns after the first clock delay, after the last WRITE is executed.

11. Precharge mode only.

SDRAM AC FUNCTIONAL CHARACTERISTICS (NOTES 1,2,3,4,5,6)

Parameter/Condition		Symbol	-100	-125	Units
READ/WRITE command to READ/WRITE command (10)		t_{CCD}	1	1	t_{CK}
CKE to clock disable or power-down entry mode (7)		t_{CKED}	1	1	t_{CK}
CKE to clock enable or power-down exit setup mode (7)		t_{PED}	1	1	t_{CK}
DQM to input data delay (10)		t_{DQD}	0	0	t_{CK}
DQM to data mask during WRITEs		t_{DQM}	0	0	t_{CK}
DQM to data high-impedance during READs		t_{DQZ}	2	2	t_{CK}
WRITE command to input data delay (10)		t_{DWD}	0	0	t_{CK}
Data-in to ACTIVE command (8)		t_{DAL}	4	5	t_{CK}
Data-in to PRECHARGE command (9)		t_{DPL}	2	2	t_{CK}
Last data-in to burst STOP command (10)		t_{BDL}	1	1	t_{CK}
Last data-in to new READ/WRITE command (10)		t_{CDL}	1	1	t_{CK}
Last data-in to PRECHARGE command (9)		t_{RDL}	2	2	t_{CK}
LOAD MODE REGISTER command to ACTIVE or REFRESH command (11)		t_{MRD}	2	2	t_{CK}
Data-out to high-impedance from PRECHARGE command (10)	CL = 3	t_{ROH}	3	3	t_{CK}
	CL = 2	t_{ROH}	2	—	t_{CK}

NOTES:

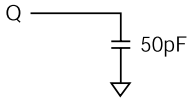
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.

2. An initial pause of 100ms is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VCC must be powered up simultaneously.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.

3. AC characteristics assume tT = 1ns.

4. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.

5. Outputs measured at 1.5V with equivalent load:



6. AC timing and ICC tests have VIL = 0V and VIH = 3V, with timing referenced to 1.5V crossover point.

7. Timing actually specified by tCKS; clock(s) specified as a reference only at minimum cycle rate.

8. Timing actually specified by tWR plus tRP; clock(s) specified as a reference only at minimum cycle rate.

9. Timing actually specified by tWR.

10. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.

11. JEDEC and PC100 specify three clocks.

both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the JEDEC Single-Power-Supply Flash Standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and program circuitry. Write cycles also internally latch addresses and data needed for the programming circuitry. Write cycles also internally latch addresses abd data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the Embedded Program algorithm – an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The Unlock Bypass mode faciclitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the Embedded Erase algorithm – an internal algorithm that automaticaally preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether as program or erase operation is complete by observing the RY/BY1 pin, or by reading $\overline{FD7}$ (Data Polling) and FD6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The Sector Erase Architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectords. The device is fully erased when shipped from the factory.

Hardware Data Protection measures include a low Vcc detector that automatically inhibits write operations during power transitions. The Hardware Sector Protection feature disables bith program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Hardware Sector Protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend feature enables the user to put erase on hold for any period of time to read data from, or proThe gram data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The Hardware Rest ($\overline{RST}$) pin terminates any operation in progress and resets the internal state machine to reading array data. The $\overline{RST}$ pin may be tied to the reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from Flash memory.

The device offers two power saving features. When addresses have been stable for specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 4 lists the device bus operations, the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

WORD/BYTE CONFIGURATION

The $\overline{BYTE1}$ pin controls whether the device data I/O pins $\overline{FDO-15}$ operate in the byte or word configuration. If the $\overline{BYTE1}$ pin is set at logic '1', the device is in word configuration, FD0-15 are active and controlled by $\overline{FCS}$ and $\overline{FOE}$.

If the BYTE1 pin is set at logic '0', the device is in byte configuration, and only data I/O pins FD0-7 are active and controlled by $\overline{FCS}$ and $\overline{FOE}$. The data I/O pins FD8-14 are tri stated, and the FD15 pin is used as an input for the LSB (FA-1) address function.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the $\overline{FCS}$ and $\overline{FOE}$ pins to VIL. $\overline{FCS}$ is the power control and selects the device. $\overline{FOE}$ is the output control and gates array data to the output pins. FWE should remain at VIH. The $\overline{BYTE1}$ pin determines whether the device outputs array data in words or bytes.

TABLE 4 - DEVICE BUS OPERATIONS

Operation	$\overline{FCS}$	$\overline{FOE}$	$\overline{FWE}$	$\overline{RST}$	Addresses (2)	FD_{0-7}	FD_{8-15}	
							$\overline{BYTE1}$ = V_{IH}	$\overline{BYTE1}$ = V_{IL}
Read	L	L	H	H	FA_{IN}	FD_{OUT}	FD_{OUT}	FD_{8-14} = High Z
Write	L	H	L	H	FA_{IN}	FD_{OUT}	FD_{OUT}	FD_{15} = FA_{-1}
Standby	Vcc ±0.3V	X	X	Vcc ± 0.3V	X	High Z	High Z	High Z
Output Disable	L	H	H	H	X	High Z	High Z	High Z
Reset	X	X	X	L	X	High Z	High Z	High Z
Sector Protect (1)	L	H	L	V_{ID}	Sector Address, FA_6 = L, FA_1 = H, FA_0 = L	FD_{IN}	X	X
Sector Unprotect (1)	L	H	L	V_{ID}	Sector Address, FA_6 = H, FA_1 = H, FA_0 = L	FD_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	FD_{IN}	FD_{IN}	High Z

LEGEND:

L = Logic Low = VIL *X = Don't Care* *FDOUT = Flash Data Out*

H = Logic High = VIH *FAIN = Flash Address In*

VID = 12.0 ± 0.5V *FDIN = Flash Data In*

NOTES:

1. The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.

2. Addresses are FA18: FA0 in word mode (BYTE1 = V_{IH}), FA18: FA-1 in byte mode (BYTE1 = V_{IL})

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that not spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the Flash AC Read-only Operations table for timing specifications and to Figure 11 for the timing diagram. IFCC1 in the ICC Specifications and Conditions table represents the active current specification for reading array data.

WRITE COMMANDS/COMMAND SEQUENCES

To writes a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive $\overline{FWE}$ and $\overline{FCS}$ to VIL, and $\overline{FOE}$ to VIH.

For program operations, the $\overline{BYTE1}$ pin determines whether the device accepts program data in bytes or words. Refer to "Word/Byte Configuration" for more information.

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a byte, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 5 indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Flash Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on FD7-0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

IFCC2 in the DC Characteristics table represents the active current specifications for the write mode. The "Flash AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

PROGRAM AND ERASE OPERATION STATUS

During an erase or program operation, the system may check the status of the operation by reading the status bits on FD7-

0. Standard read cycle timings and IFCC read specifications apply. Refer to "Write Operation Status" for more information, and to "Flash AC Characteristics" for timing diagrams.

STANDBY MODE

When the system is not reading or writing to the device, it can place the device in standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the $\overline{FOE}$ input.

The device enters the CMOS standby mode when the $\overline{FCS}$ and $\overline{RST}$ pins are both held at Vcc ±0.3V. (Note that this is a more restricted voltage range than VIH.) If $\overline{FCS}$ and $\overline{RST}$ are held at VIH, but not within Vcc to ±0.3V the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the Flash DC Characteristics table, IFCC3 and IFCC4 represent the standby current specifications.

AUTOMATIC SLEEP MODE

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the $\overline{FCS}$, $\overline{FWE}$, and $\overline{FOE}$ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Ifcc5 in the DC Characteristics table represents the automatic sleep mode current specification.

$\overline{RST}$: HARDWARE RESET PIN

The $\overline{RST}$ pin provides a hardware method of resetting the device to reading array data. When the $\overline{RST}$ pin is driven low for at least a period of tRP or greater the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the $\overline{RST}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the $\overline{RST}$ pulse. When

TABLE 5 - BOTTOM BOOT BLOCK SECTOR ADDRESS TABLE

Sector	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes)	(x8) Address Range (In hexidecimal)
SA0	0	0	0	0	0	0	X	16	00000h-03FFFh
SA1	0	0	0	0	0	1	0	8	04000h-05FFFh
SA2	0	0	0	0	0	1	1	8	06000h-07FFFh
SA3	0	0	0	0	1	X	X	32	08000h-0FFFFh
SA4	0	0	0	1	X	X	X	64	10000h-1FFFFh
SA5	0	0	1	0	X	X	X	64	20000h-2FFFFh
SA6	0	0	1	1	X	X	X	64	30000h-3FFFFh
SA7	0	1	0	0	X	X	X	64	40000h-4FFFFh
SA8	0	1	0	1	X	X	X	64	50000h-5FFFFh
SA9	0	1	1	0	X	X	X	64	60000h-6FFFFh
SA10	0	1	1	1	X	X	X	64	70000h-7FFFFh
SA11	1	0	0	0	X	X	X	64	80000h-8FFFFh
SA12	1	0	0	1	X	X	X	64	90000h-9FFFFh
SA13	1	0	1	0	X	X	X	64	A0000h-AFFFFh
SA14	1	0	1	1	X	X	X	64	B0000h-BFFFFh
SA15	1	1	0	0	X	X	X	64	C0000h-CFFFFh
SA16	1	1	0	1	X	X	X	64	D0000h-DFFFFh
SA17	1	1	1	0	X	X	X	64	E0000h-EFFFFh
SA18	1	1	1	1	X	X	X	64	F0000h-FFFFFh

$\overline{RST}$ is held at Vss ± 0.3V, the device draws CMOS standby current (IFCC4). If $\overline{RST}$ is held at VIL but not within Vss ± 0.3V, the standby current will be greater.

The $\overline{RST}$ pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If $\overline{RST}$ is asserted during a program or erase operation, RY/$\overline{BY1}$ pin remains "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/$\overline{BY1}$ to determine whether the reset operationis complete. If $\overline{RST}$ is asserted when a program or erase operation is not executing (RY/$\overline{BY1}$ pin is "1"), the reset operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the $\overline{RST}$ pin returns to VIH.

Refer to the Flash AC Characteristics and hardware reset tables for $\overline{RST}$ parameters and to Figure 19 for the timing diagram.

AUTOSELECT MODE

The autoselect mode provides sector protection verification, through identifier codes input codes output on FD7-0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires VID (11.5V to 12.5V) on address in FA9. Address pins FA6, FA1, and FA0 must be as shown in Table 6. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 5). Table 6 shows the remaining address bits that are "don't care." When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on FD7-0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 7. This method does not require VID. See "Command Definitions" for details on using the autoselect mode.

SECTOR PROTECTION/ UNPROTECTION

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

This operation requires VID on the RST pin only, and can be implemented either in-system or via programming equipment. Figure 5 shows the algorithms and the timing diagram is shown in figure 18. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

TEMPORARY SECTOR UNPROTECT

This feature allows temporary unprotection of previously protected sector groups to change data-in system. The Sector Unprotect mode is activated by setting the RST pin to VID. During this mode, formerly protected sector can be programmed or erased by selecting the sector addresses. Once VID is removed from the RST pin, all the previously protected sector groups will be protected again. Figure 16 shows the algorithm and the timing diagram is shown in Figure 17, for this feature.

HARDWARE DATA PROTECTION

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 7 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during Vcc power-up and power-down transitions, or from system noise.

Low Vcc Write Inhibit

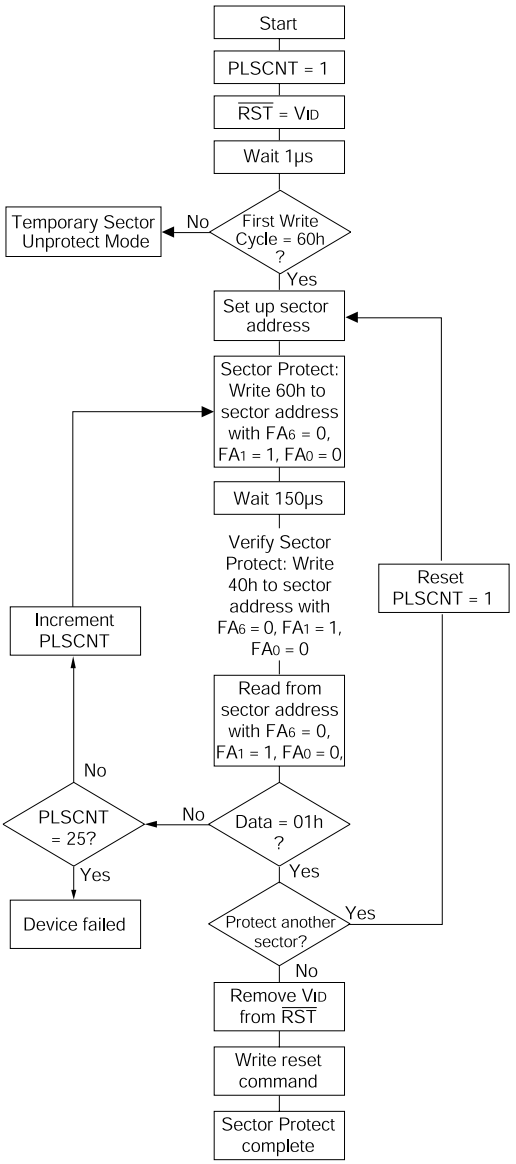
When Vcc is less than VLKO, the device does not accept any write cycles. Ths protects data during Vcc power-up and

Table 6 - Autoselect Codes (High Voltage Method)

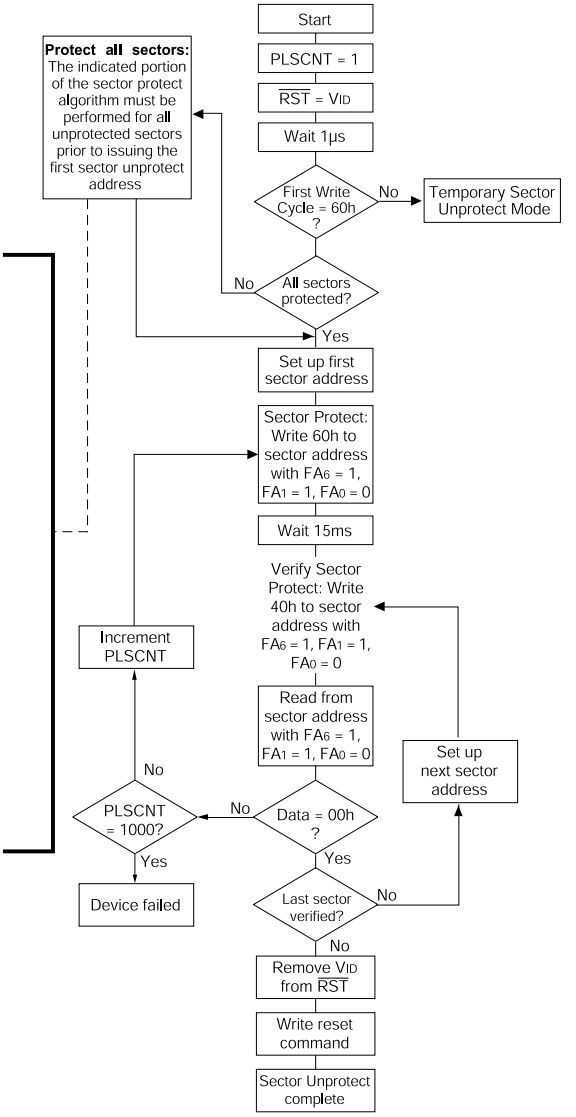
Description	$\overline{FCS}$	$\overline{FOE}$	$\overline{FWE}$	FA18-12	FA11-10	FA9	FA8-7	FA6	FA5-2	FA1	FA0	FD7-0
Sector Protection Verificaton	L	L	H	SA	X	VID	X	L	X	H	L	01h (protected)
												00h (unprotected)

L = Logic Low = VIL, H = Logic High = VIH, SA = Sector Address, X = Don't Care

FIG. 5 SECTOR PROTECT/UNPROTECT ALGORITHMS



SECTOR PROTECT ALGORITHM



SECTOR UNPROTECT ALGORITHM

power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until Vcc is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than VLKO.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{FOE}$, $\overline{FCS}$, or $\overline{FWE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{FOE}$ = VIL, $\overline{FCS}$ = VIH or $\overline{FWE}$ = VIH. To initiate a write cycle, $\overline{FCS}$ and $\overline{FWE}$ must be a logical zero while $\overline{FOE}$ is a logical one.

Power-Up Write Inhibit

If $\overline{FWE}$ = $\overline{FCS}$ = VIL and $\overline{FOE}$ = VIH during power up, the device does not accept commands on the rising edge of $\overline{FWE}$. The internal state machine is automatically reset to reading array data on power-up.

FLASH COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 7 defines the valid register command sequences. **Writing incorrect address and data values or writing them in improper sequence will reset the device to the read array data**.

All addresses are latched on falling edge of $\overline{FWE}$ or $\overline{FCS}$, whichever occurs later. All data is latched on the rising edge of $\overline{FWE}$ or $\overline{FCS}$, whichever occurs first. Refer to the appropriate timing diagrams in the "Flash AC Characteristics" section.

READ ARRAY DATA

Upon initial device power-up the device defaults to read array data. No commands are required to retrieve data. The device is also ready to read array data after it has completed an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspend sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if FD5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" on the "Bus Operations" section for more information. The Data Sheet Read Operations table provides the read parameters, and the Read Operations Timing Diagram shows the timing diagram.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are "don't care" for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

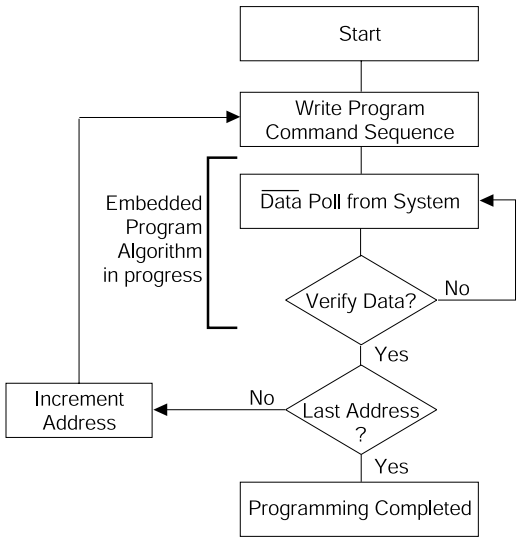
The reset command may be written between the sequence cycles in an autoselect command sequence. Once in autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend mode).

If FD5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in fast total programming time. Table 7 shows the requirements for the com-

FIG. 6 PROGRAM OPERATION



NOTE: See Table 7 for program command sequence.

mand sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are "don't care" for both cycles. The device then returns to reading array data.

Figure 6 illustrates the algorithm for the program operation. See the Erase/Program Operations table in the "Flash AC Characteristics" for parameters, and to Figure 12 for timing diagrams.

AUTOSELECT COMMAND SEQUENCE

The autoselect command sequence allows the host system to determine whether or not a sector is protected. Table 7 shows the address and data requirements. This method is an alternative to that shown in Table 6, which is intended for PROM programmers and requires V_{ID} on address bit FA9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 02h in that sector is protected, or 00h if it is unprotected. Refer to Table 5 for valid sector addresses.

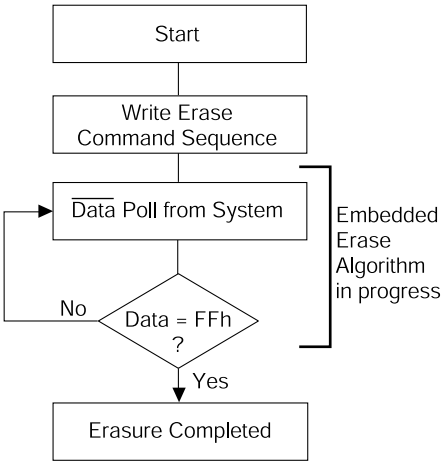
The system must write the reset command to exit autoselect mode and return to reading array data.

WORD/BYTE PROGRAM COMMAND SEQUENCE

The system may program the device by word or byte, depending on the state of the $\overline{BYTE1}$ pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timing. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 7 shows the address and data requirements for the byte program command sequence.

When the Embedded program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using FD7, FD6, or RY/$\overline{BY1}$. See "Write Operation Status" for information on these status bits.

FIG. 7 ERASE OPERATION



1. See Table 5 for erase command sequence.
2. See "FD3 : Sector Erase Timer" for more information.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The program command sequences should be reinitiated once the device has reset to reading array data, to ensure date integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set FD5 to "1", or cause the Data Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

CHIP ERASE COMMAND SEQUENCE

Chip erase is six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a setup command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 7 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be re-initiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using FD7, FD6, or FD2, or RY/BY1. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 7 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "Flash AC Characteristics" for parameters, and to Figure 13 for timings diagram.

SECTOR ERASE COMMAND SEQUENCE

Sector erase is six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a setup command. Two additional unlock write cycles are then followed by the address of the

sector to be erased, and the sector erase command, which in turn invokes the Embedded Erase algorithm. Table 7 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.After the command sequence is written, a sector erase time-out of 50µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50µs, the system need not monitor FD3. **Any command other than the Sector Erase or Erase Suspend during the time-out period resets the device to reading array data**. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor FD3 to determine if the sector erase timer has timed out. See the "FD3: Sector Erase Timer" section. The time-out begins from the rising edge of the final $\overline{FWE}$ pulse in command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other command is valid. All other commands are ignored. Note that a hardware reset during the sector erase operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using FD7, FD6, or FD2, or RY/$\overline{BY1}$. See "Write Operation Status" for information on these status bits.

Figure 7 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in the "Flash AC Characteristics" for parameters, and to Figure 13 for timings diagram.

ERASE SUSPEND/ERASE RESUME COMMAND SEQUENCE

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on FD7-0. The system can use FD7, or FD6, and FD2 together, to determine if a sector is actively erasing or is erase suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the FD7 or FD6 status bits, just as in the standard program operation. See the "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

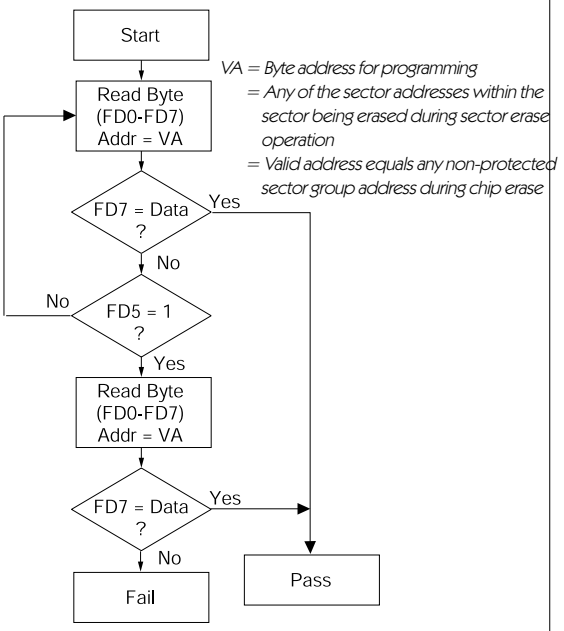
TABLE 7 - COMMAND DEFINITIONS

Command Sequence (Note 1)			Bus Write Cycles Req'd	Bus Cycles (Notes 2, 3, 4, 13)											
				First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)			1	RA	RD										
Reset (Note 6)			1	XXX	F0										
Autoselect	Device ID, Bottom Boot Block	Byte	4	AAA	AA	555	55	AAA	90	X02	5B				
		Word		555		2AA		555		X01	225B				
	Sector Protect Verify (Note 7,8)	Byte	4	AAA	AA	555	55	AAA	90	(SA) X04	XX00 01				
		Word		555		2AA		555		(SA) X02	XX00 XX01				
Program		Byte	4	AAA	AA	555	55	AAA	A0	PA	PD				
		Word		555		2AA		555							
Unlock Bypass		Byte	3	AAA	AA	555	55	AAA	20						
		Word		555		2AA		555							
Unlock Bypass Program (Note 9)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note10)			2	XXX	90	PA	00								
Chip Erase		Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
		Word		555		2AA		555		555		2AA		555	
Sector Erase		Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
		Word		555		2AA		555		555		2AA			
Erase Suspended (Note 11)			1	XXX	B0										
Erase Resume (Note 12)			1	XXX	30										

LEGEND:
X = Don't Care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{FWE}$ or $\overline{FCS}$ pulse, whichever occurs first.
PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{FWE}$ or $\overline{FCS}$ pulse, whichever occurs first.
SA = Address of the sector to be erased. The combination of FA18-12 will uniquely select any sector.

NOTES:
1. Bus operations are defined in Table 3.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operations.
4. Address bits FA18-11 = don't care for unlock and command cycles, unless PA or SA is required.
5. No unlock or command cycles required when reading array data.
6. The Reset command is required to return to reading array data when device is in the autoselect mode, or if FD5 goes high (while the device is providing status data).
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. The data is 00h for an unprotected sector and 01h for a protected sector.
9. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
10. The Unlock Bypass Reset command is required to return to reading array data when the device is in the Unlock Bypass mode.
11. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
12. The Erase Resume command is valid only during the Erase Suspend mode.
13. Data bots FD8-15 are don't cares for unlock and command cycles.

FIG. 8 DATA POLLING ALGORITHM



1. FD7 should be rechecked even if FD5 = 1 because FD7 may change simultaneously with FD5.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: FD2, FD3, FD5, FD6, and FD7. Table 8 and the following subsections describe the functions of these bits. FD7, RY/$\overline{BY1}$, and FD6 each offer a method for determining whether a program or erase operation is complete or in progress. These bits are discussed first.

FD7: $\overline{\text{DATA}}$ POLLING

The $\overline{\text{Data}}$ Polling bit, FD7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend $\overline{\text{Data}}$ Polling valid after the rising edge of the final $\overline{\text{FWE}}$ pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on FD7 the complement of the datum programmed to FD7. This FD7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to FD7. The system must provide the program address to read valid status information on FD7. If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on FD7 is active for approximately 1μs, then the device returns to reading array data.

During the Embedded Erase algorithm, $\overline{\text{Data}}$ Polling produces a "0" on FD7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, $\overline{\text{Data}}$ Polling produces a "1" on FD7. This analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on FD7.

After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on FD7 is active for approximately 100μs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects FD7 has changed from the complement to true data, it can read valid data at FD7-0 on the *following* read cycles. This because FD7 may change asynchronously with FD0-6 while Flash Output Enable ($\overline{\text{FOE}}$) is asserted low. Figure 14, $\overline{\text{Data}}$ Polling timings (During Embedded algorithms), in the "Flash AC characteristics" section illustrates this.

Table 8 shows the outputs for $\overline{\text{Data}}$ Polling on FD7. Figure 8 shows the $\overline{\text{Data}}$ Polling algorithm.

RY/$\overline{BY1}$: READY/$\overline{BUSY}$

The RY/$\overline{BY1}$ is a dedicated, open drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/$\overline{BY1}$ status is valid after the rising edge of the final $\overline{FWE}$ pulse in the command sequence. Since RY/$\overline{BY1}$ is an open-drain output, several RY/$\overline{BY1}$ pins can be tied together in parrallel with a pull-up resistor to Vcc.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode.), or is in the standby mode.

Table 8 shows the outputs for RY/$\overline{BY1}$. Figures 11, 12, 13, 19 show RY/$\overline{BY1}$ for read, program, erase and reset operations, respectively.

FD6: TOGGLE BIT I

"Toggle Bit I" on FD6 indicates whether an Embedded Program or Erase Algorithm is in progress or has been completed, or whether the device has entered the Erase Suspend mode. Toggle Bit I may read at any address, and is valid after the rising edge of the final $\overline{FWE}$ pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase Algorithm operation, successive read cycles to any address will result in FD6 toggling. (The system may use either $\overline{FOE}$ or $\overline{FCS}$ to control the read cycles.) When operation is complete, FD6 stops toggling.

After the erase command sequence is written, if all selectors selected for erasing are protected. FD6 toggles for approximately 100μs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase Algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use FD6 and FD2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase Algorithm is in progress) FD6 toggles. When the device enters the Erase Suspend mode, FD6 stops toggling. However, the system must also use FD2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use FD7 (see the subsection on "FD7: Data Polling").

If a program address falls within a protected sector, FD6 also toggles for approximately 1μs after the program command sequence is written, then returns to reading array data. FD6 also toggles during erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 8 shows the outputs for "Toggle Bit I" on FD6. Figure 9 shows the Toggle Bit Algorithm. Figure 21 shows the toggle bit timing diagrams. Figure 20 shows the difference between FD2 and FD6 in graphical form. See also the subsection on "FD2: Toggle Bit II".

FD2: TOGGLE BIT II

The "Toggle Bit II" on FD2, when used with FD6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase Algorithm is in progress) or whether that sector is erase-suspended. "Toggle Bit II" is valid after the rising edge of the final FWE pulse in the command sequence.

FD2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either FOE or FCS to control the read cycles.) FD2 cannot distinguish whether the sector is actively erasing or is erase-suspended. FD6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 8 to compare outputs for FD2 and FD6.

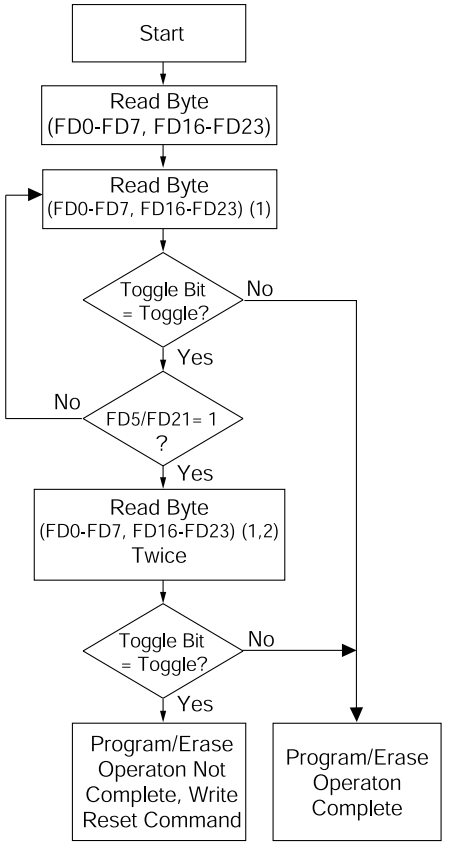
Figure 9 shows the Toggle Bit Algorithm in flowchart form, and the section "FD2: Toggle Bit II" explains the algorithm. See also the subsection on "FD6: Toggle Bit I". Figure 21 shows the toggle bit timing diagrams. Figure 20 shows the difference between FD2 and FD6 in graphical form.

READING TOGGLE BITS FD6/FD2

Refer to Figure 9 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read FD7-FD0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on FD7-0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of FD5 is high (see the section on FD5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may

FIG. 9 TOGGLE BIT ALGORITHM



1. Read toggle bit twice to detemine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as FD5 changes to 1. See text.

have stopped toggling just as the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and FD5 has not gone high. The system may continue to monitor the toggle bit and FD5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 9).

FD5: EXCEEDED TIMING LIMITS

FD5 will indicate whether the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions FD5 will produce a "1". This is a failure condition that indicates the program or erase cycle was not successfully completed.

The FD5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded timing limits, the FD5 bit will produce a "1".

Under both these conditions, the system must issue the reset command to return the device to reading array data.

FD3: SECTOR ERASE TIMER

After writing a sector erase command sequence, the system may read FD3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is completed, FD3 switches from "0" to "1." The system may ignore FD3 if the system can guarantee that the time between additional sector erase commands will always be less than 50µs. See also the "Sector Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on FD7 ($\overline{\text{Data}}$ Polling) or FD6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read FD3. If FD3 is high ("1") the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) will be ignored until the erase operation is completed. If FD3 is low ("0"), the device

will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of FD3 prior to and following each subsequent sector erase command. If FD3 is high on the second status check, the last command may not have been accepted. Table 8 shows the outputs for FD3.

TABLE 8 - WRITE OPERATION STATUS

	Status	FD7(2)	FD6	FD5(1)	FD3	FD2(2)	RY/$\overline{BY}$1
Standard Mode	Embedded Program Algorithm	$\overline{FD7}$	Toggle	0	N/A	No Toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase Suspended Program	$\overline{FD7}$	Toggle	0	N/A	N/A	0

NOTES:
1. FD5 switches to "1" when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "FD5: Exceed Timing Limits" for more information.
2. FD7 and FD2 require valid address when reading status information. Refer to the appropriate subsection for further details.

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED
(VCC = 3.3V, VSS = 0V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time	t_{WHWH2}			15		15		15	sec
Read Recovery Time (2)	t_{GHEL}		0		0		0		µs
Chip Programming Time				50		50		50	sec

1. Typical value for tWHWH1 is 9µs.
2. Guaranteed by design, but not tested.

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED
(VCC = 3.3V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	50		50		65		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	50		50		65		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	50		50		65		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		30		35		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				50		50		50	sec
Output Enable Setup Time		t_{OES}	0		0		0		ns
Output Enable Hold Time (2)		t_{OEH}	10		10		10		ns

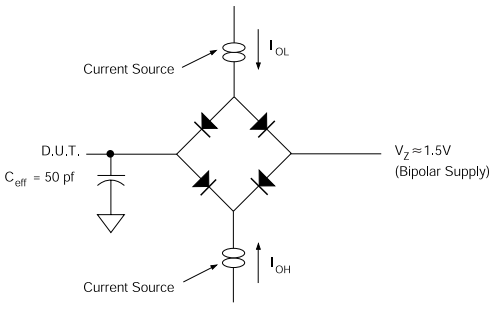
1. Typical value for tWHWH1 is 9µs.
2. For Toggle and Data Polling.
3. Guaranteed by design, but not tested.

FLASH AC CHARACTERISTICS – READ-ONLY OPERATIONS
(VCC = 3.3V, TA = -55°C TO +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	100		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		100		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		100		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		30		30		40	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		30		30		40	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns

1. Guaranteed by design, not tested.

FIG. 10 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 11 FLASH AC WAVEFORMS FOR READ OPERATIONS

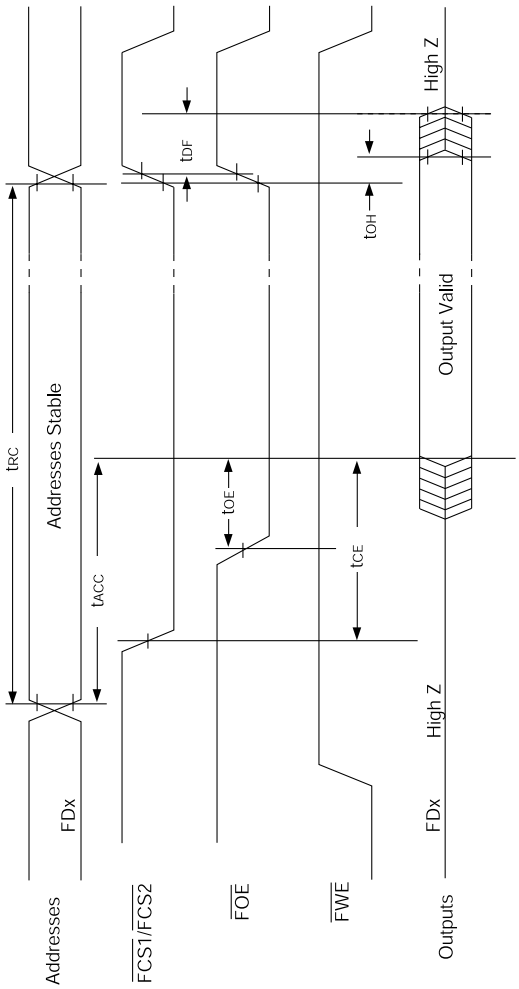
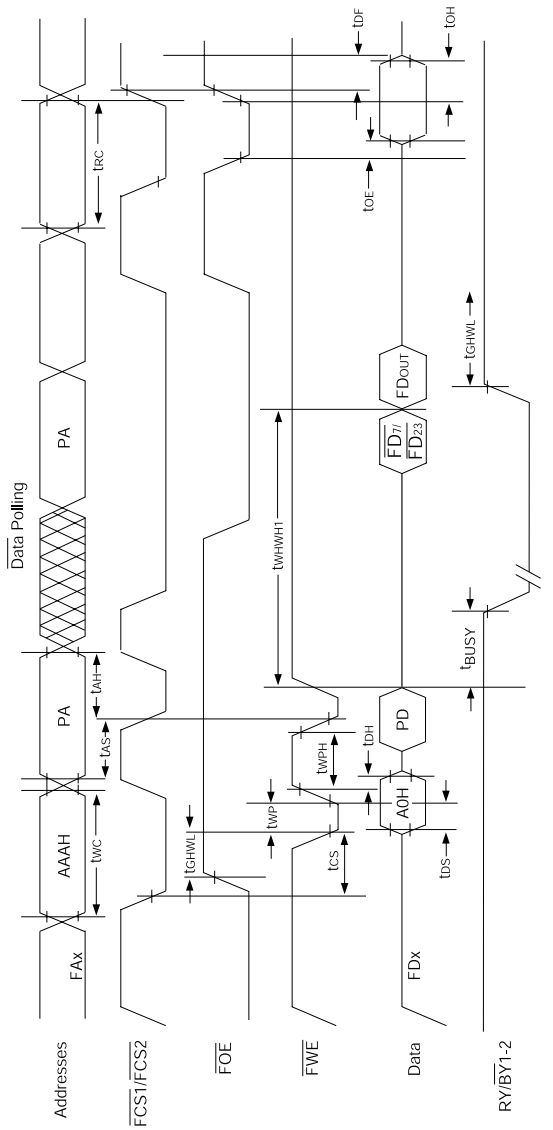


FIG. 12 FLASH WRITE/ERASE/PROGRAM OPERATION, $\overline{FWE}$ CONTROLLED



NOTES:

1. PA is the address of the memory location to be programmed.

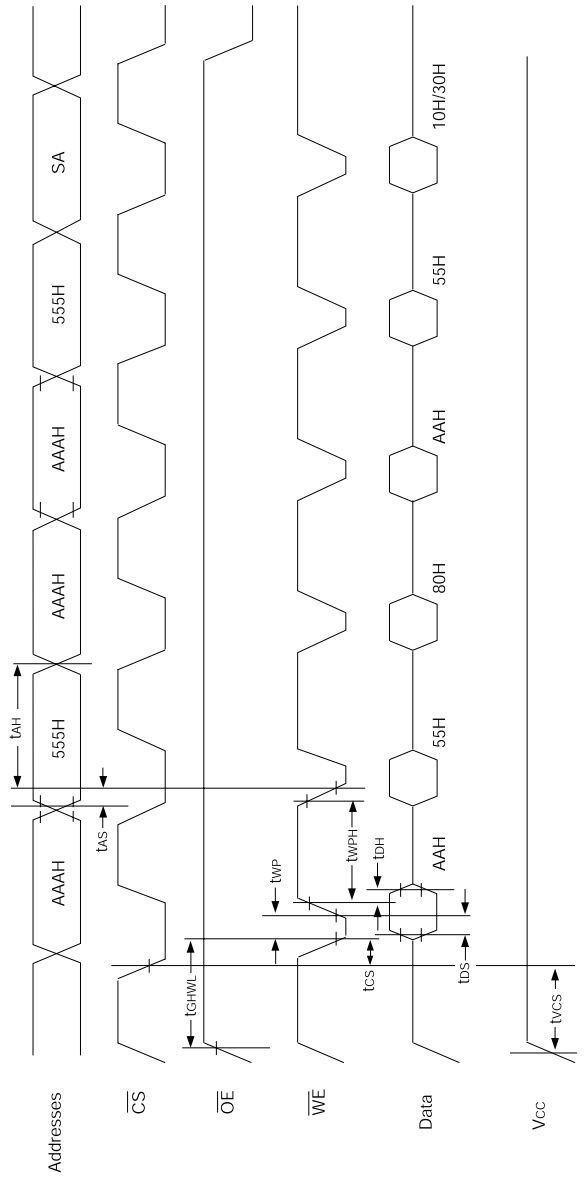
2. PD is the data to be programmed at byte address.

3. $\overline{FD7}$ is the output of the complement of the data written to each chip.

4. FDOUT is the output of the data written to the device.

5. Figure indicates last two bus cycles of four bus cycle sequence.

FIG. 13 FLASH AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.

FIG. 14 FLASH AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

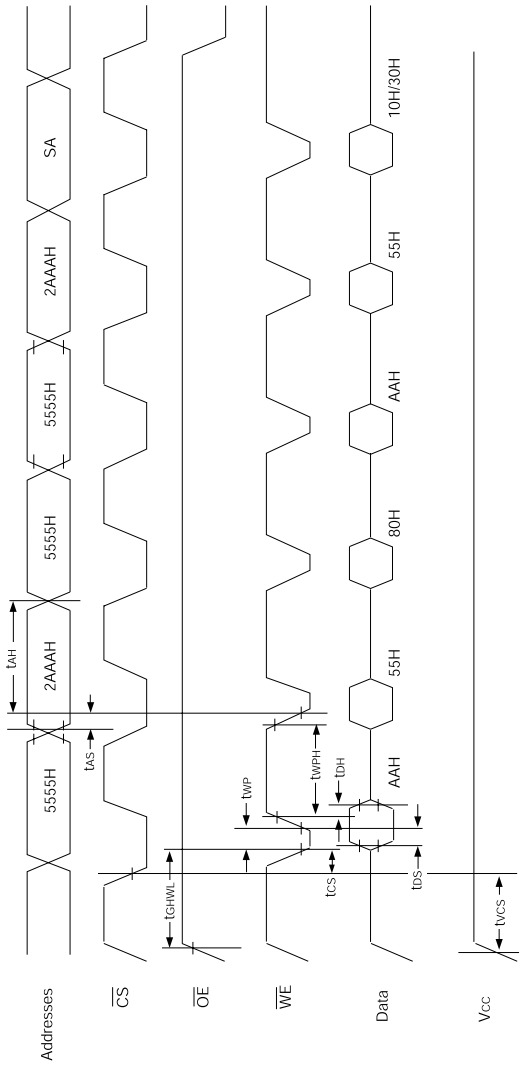
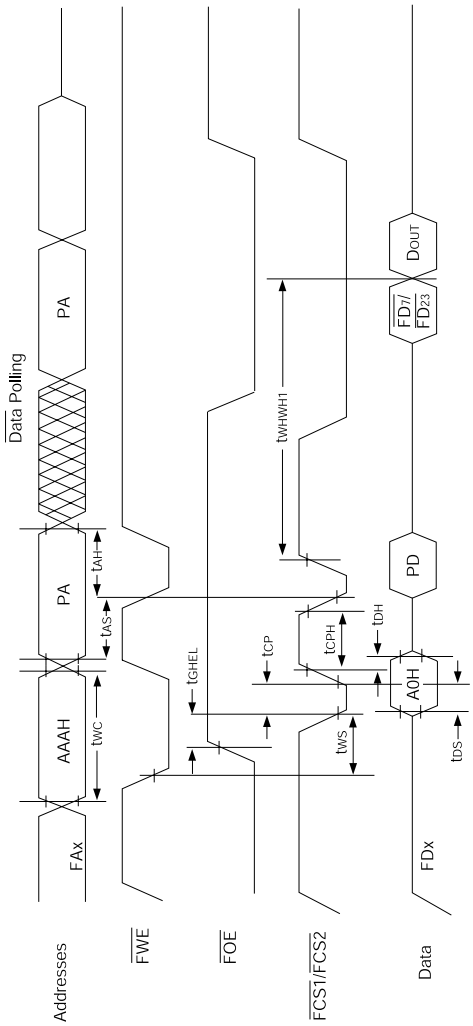


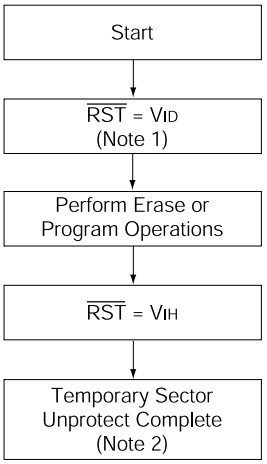
FIG. 15 FLASH ALTERNATE $\overline{FCS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS



Notes:

1. *FPA represents the address of the memory location to be programmed.*
2. *PD represents the data to be programmed at byte address.*
3. *$\overline{FD7}$ is the output of the complement of the data written to each chip.*
4. *FDOUT is the output of the data written to the device.*
5. *Figure indicates the last two bus cycles of a four bus cycle sequence.*

FIG. 16 TEMPORARY SECTOR UNPROTECT OPERATION



1. All protected sectors unprotected.
2. All previously protected sectors are protected once again.

FIG. 17 TEMPORARY SECTOR UNPROTECT TIMING DIAGRAM

Parameter	Description		All Speed Options	Unit
t_{VIDR}	Vid Rise and Fall Time (See Note)	Min	500	ns
t_{RSP}	RST Setup Time for Temporary Sector Unprotect	Min	4	µs

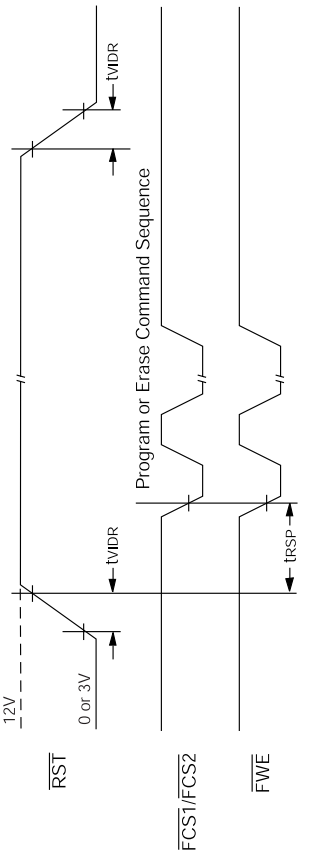
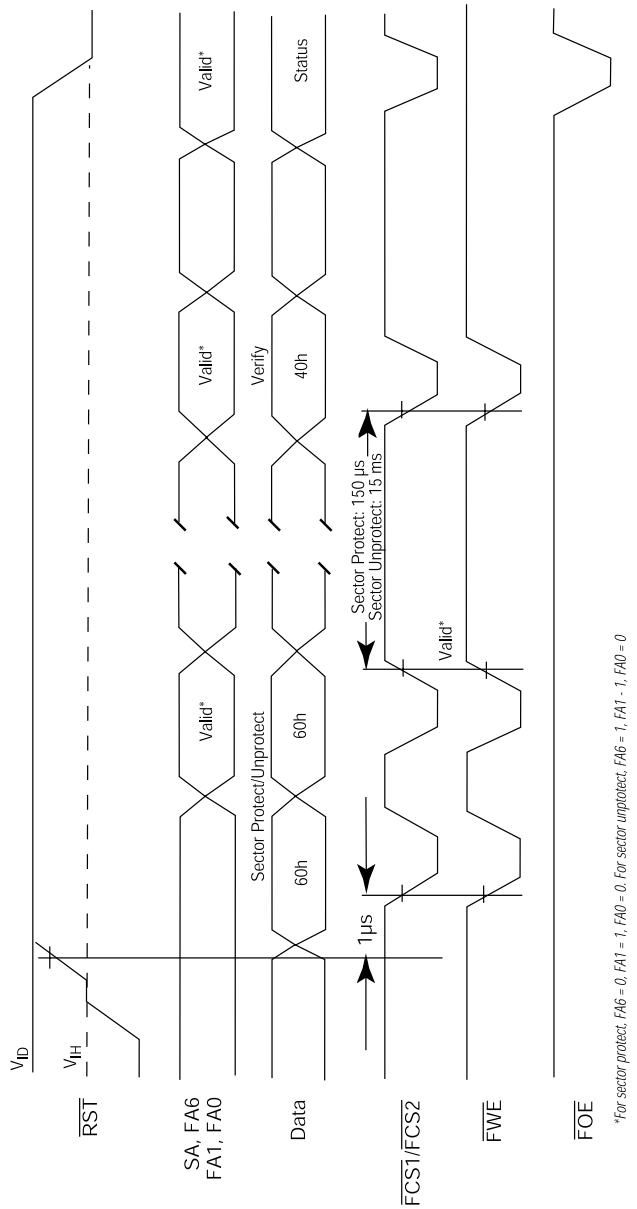


FIG. 18 AC CHARACTERISTICS SECTOR PROTECT/UNPROTECT TIMING DIAGRAM



Parameter	Description	Test Setup	All Speed Options	Unit
t_{Ready}	$\overline{RST}$ Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	µs
t_{Ready}	$\overline{RST}$ Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
t_{RP}	$\overline{RST}$ Pulse Width	Min	500	ns
t_{RH}	$\overline{RST}$ High Time Before Read (See Note)	Min	50	ns
t_{RPD}	$\overline{RST}$ Low to Standby Mode	Min	20	µs
t_{RB}	RY/$\overline{BY1}$ Recovery Time	Min	0	ns

Note:
Not 100% tested.

FIG. 19 HARDWARE RESET ($\overline{RST}$)

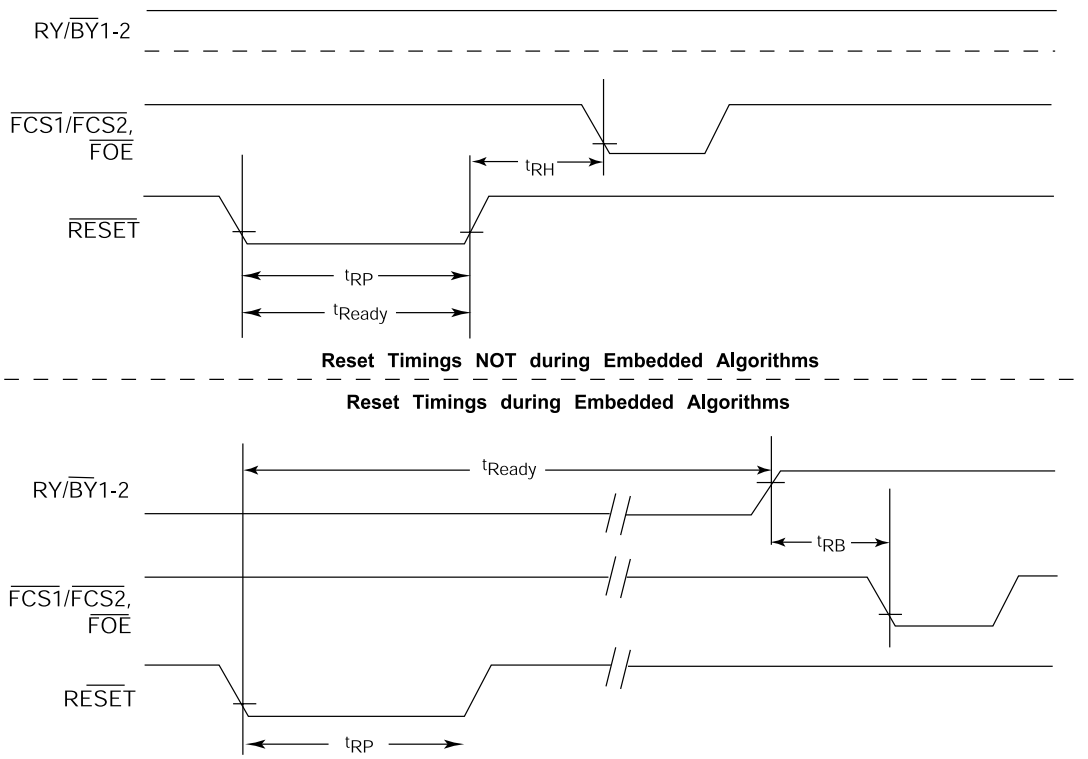
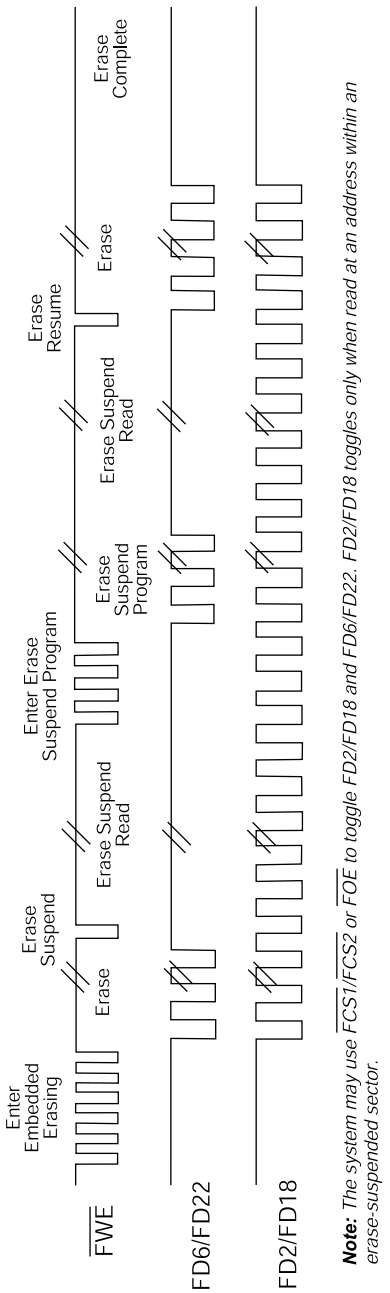
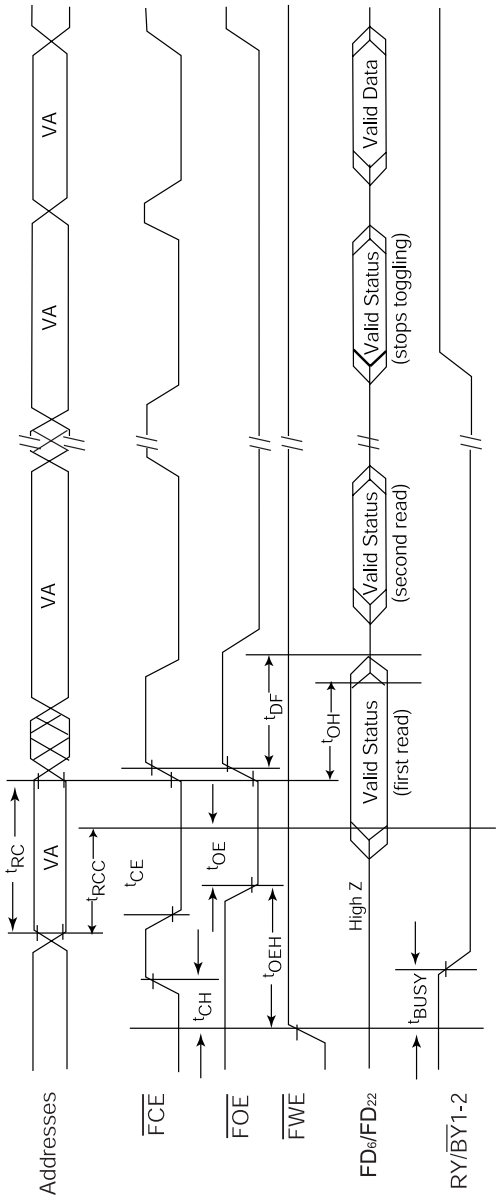


FIG. 20 AC CHARACTERISTICS DQ 2 VS. DQ 6



Note: *The system may use $\overline{FCS1}$/$\overline{FCS2}$ or $\overline{FOE}$ to toggle FD2/FD18 and FD6/FD22. FD2/FD18 toggles only when read at an address within an erase-suspended sector.*

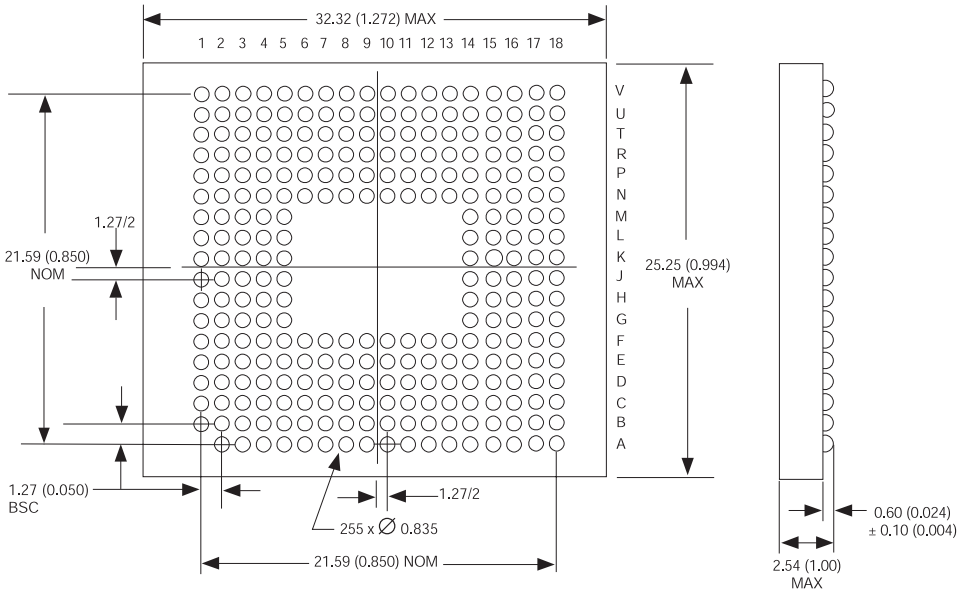
FIG. 21 TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



Note: VA = Valid address; not required for FD6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

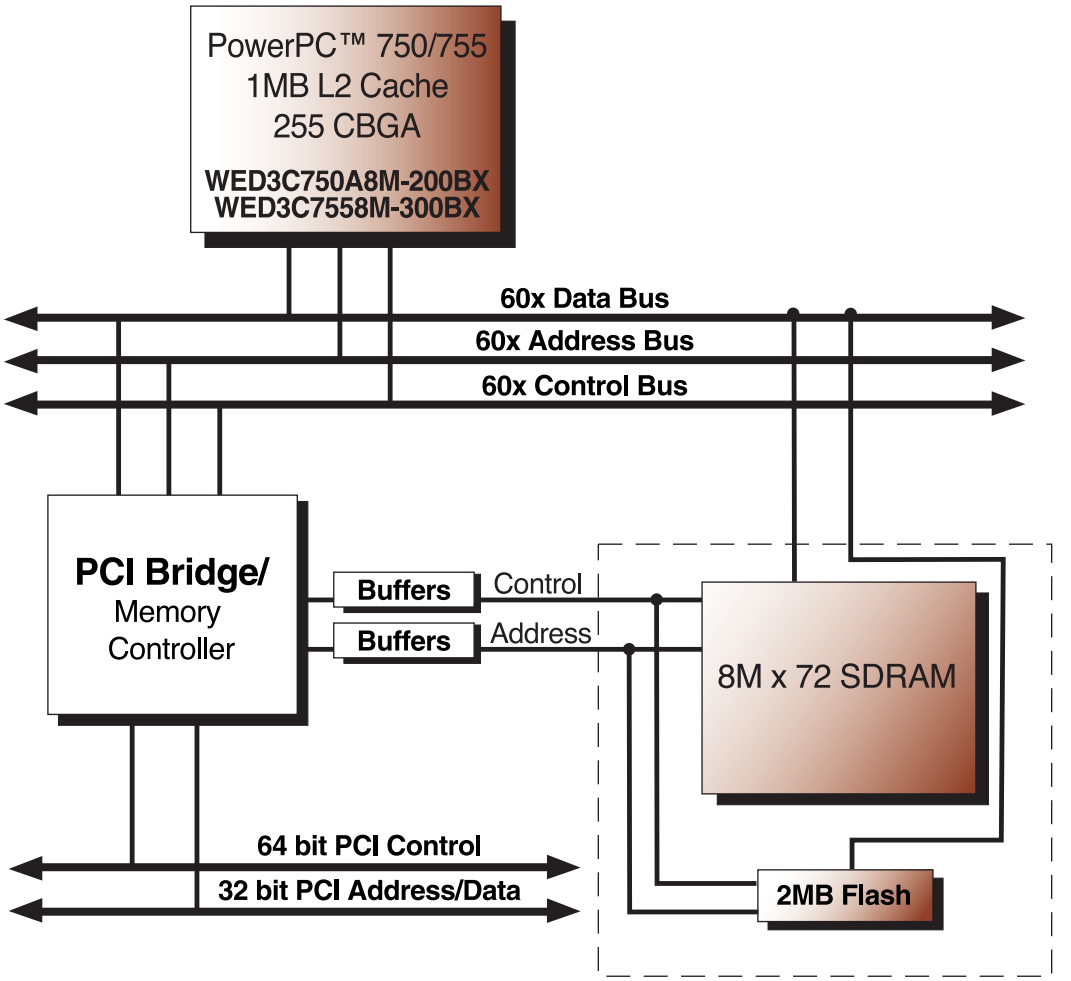
PACKAGE 743: 275 PLASTIC BALL GRID ARRAY (PBGA)

BOTTOM VIEW



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

750 PowerPC™ System Block Diagram



ORDERING INFORMATION

WED P N F 8M 72 1 V - XXXX B X

DEVICE GRADE:

M	= Military	-55°C to +125°C
I	= Industrial	-40°C to +85°C
C	= Commercial	0°C to +70°C

PACKAGE:

B = 275 Plastic Ball Grid Array (PBGA)

FREQUENCY (MHz)

1010 = 100MHz SDRAM/100ns Flash
1012 = 100MHz SDRAM/120ns Flash
1015 = 100MHz SDRAM/150ns Flash
1210 = 125MHz SDRAM/100ns Flash
1212 = 125MHz SDRAM/120ns Flash
1215 = 125MHz SDRAM/150ns Flash

3.3V Power Supply

Flash CONFIGURATION, 1M x 8/512K x 16 (1MB)

SDRAM CONFIGURATION, 8M x 72 (64MB)

FLASH

SDRAM

PLASTIC

WHITE ELECTRONIC DESIGNS CORP.