# 512Kx32 SRAM MULTI-CHIP PACKAGE *ADVANCED**

## FEATURES

- Access Times of 12, 15, 17, 20, ns
- Packaging
  - 16mm x 18mm, 143 PBGA
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS

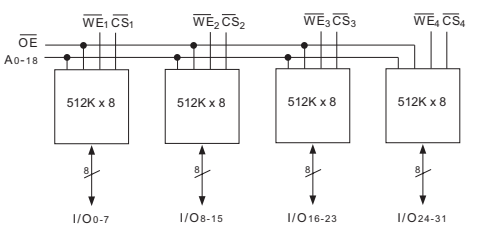
**This data sheet describes a product that is developmental, is not qualified and is subject to change or cancellation without notice.*

FIG. 1 **PIN CONFIGURATION FOR WEDPS512K32-XBX**

**TOP VIEW**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | - | A2 | A1 | A0 | GND | GND | Vcc | Vcc | A18 | A17 | A16 | GND |
| B | $\overline{CS2}$ | A3 | A4 | D14 | D15 | NC | $\overline{CS4}$ | D24 | D25 | $\overline{OE}$ | A15 | NC |
| C | D9 | D8 | NC | D12 | D13 | GND | Vcc | D26 | D27 | $\overline{WE4}$ | D31 | D30 |
| D | D10 | D11 | GND | GND | GND | GND | Vcc | Vcc | Vcc | Vcc | D28 | D29 |
| E | $\overline{WE2}$ | GND | GND | GND | GND | GND | Vcc | Vcc | Vcc | Vcc | Vcc | NC |
| F | GND | GND | GND | GND | GND | GND | Vcc | Vcc | Vcc | Vcc | Vcc | Vcc |
| G | Vcc | Vcc | Vcc | Vcc | Vcc | Vcc | GND | GND | GND | GND | GND | GND |
| H | $\overline{CS1}$ | Vcc | Vcc | Vcc | Vcc | Vcc | GND | GND | GND | GND | GND | NC |
| J | D1 | D0 | Vcc | Vcc | Vcc | Vcc | GND | GND | GND | GND | D23 | D22 |
| K | D2 | D3 | NC | D7 | D5 | Vcc | GND | D17 | D16 | $\overline{CS3}$ | D20 | D21 |
| L | $\overline{WE1}$ | A6 | A5 | D6 | D4 | NC | $\overline{WE3}$ | D19 | D18 | A14 | A13 | NC |
| M | GND | A7 | A8 | A9 | Vcc | Vcc | GND | GND | A10 | A11 | A12 | Vcc |

### BLOCK DIAGRAM




### PIN DESCRIPTION

| | |
|---|---|
| I/O0-31 | Data Inputs/Outputs |
| A0-18 | Address Inputs |
| $\overline{WE}$1-4 | Write Enables |
| $\overline{CS}$1-4 | Chip Selects |
| $\overline{OE}$ | Output Enable |
| Vcc | Power Supply |
| GND | Ground |
| NC | Not Connected |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -55 | +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 | +150 | °C |
| Signal Voltage Relative to GND | $V_G$ | -0.5 | Vcc+0.5 | V |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | $V_{CC}$ | -0.5 | 7.0 | V |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | Data I/O | Power |
|---|---|---|---|---|---|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | H | H | Out Disable | High Z | Active |
| L | X | L | Write | Data In | Active |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.5 | +0.8 | V |
| Operating Temp (Mil) | $T_A$ | -55 | +125 | °C |

## CAPACITANCE
## (TA = +25°C)

| Parameter | Symbol | Conditions | Max | Unit |
|---|---|---|---|---|
| $\overline{OE}$ capacitance | $C_{OE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 30 | pF |
| $\overline{WE}_{1-4}$ capacitance | $C_{WE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 10 | pF |
| $\overline{CS}_{1-4}$ capacitance | $C_{CS}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 10 | pF |
| Data I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V, f = 1.0 MHz | 10 | pF |
| Address input capacitance | $C_{AD}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 30 | pF |

*This parameter is guaranteed by design but not tested.*

## DC CHARACTERISTICS
## (VCC = 5.0V, VSS = 0V, TA = -55°C TO +125°C)

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | | 10 | µA |
| Operating Supply Current x 32 Mode | $I_{CC \times 32}$ | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, Vcc = 5.5 | | 660 | mA |
| Standby Current | $I_{SB}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, Vcc = 5.5 | | 80 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8mA | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA | 2.4 | | V |

*NOTE: DC test conditions: $V_{IH}$ = $V_{CC}$ -0.3V, $V_{IL}$ = 0.3V*

## AC CHARACTERISTICS
## (VCC = 5.0V, VSS = 0V, TA = -55°C TO +125°C)

| Parameter | Symbol | -12 | | -15 | | -17 | | -20 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Read Cycle | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 12 | | 15 | | 17 | | 20 | | ns |
| Address Access Time | $t_{AA}$ | | 12 | | 15 | | 17 | | 20 | ns |
| Output Hold from Address Change | $t_{OH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Select Access Time | $t_{ACS}$ | | 12 | | 15 | | 17 | | 20 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 7 | | 8 | | 9 | | 10 | ns |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 1 | | 2 | | 2 | | 2 | | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | $t_{CHZ}$[1] | | 7 | | 12 | | 12 | | 12 | ns |
| Output Disable to Output in High Z | $t_{OHZ}$[1] | | 7 | | 12 | | 12 | | 12 | ns |

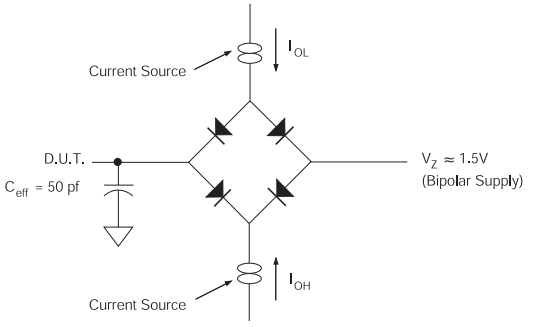
*1. This parameter is guaranteed by design but not tested.*

## AC CHARACTERISTICS
## (VCC = 5.0V, VSS = 0V, TA = -55°C TO +125°C)

| Parameter | Symbol | -12 | | -15 | | -17 | | -20 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Read Cycle | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 12 | | 15 | | 17 | | 20 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 10 | | 13 | | 15 | | 15 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 10 | | 13 | | 15 | | 15 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 8 | | 10 | | 11 | | 12 | | ns |
| Write Pulse Width | $t_{WP}$ | 10 | | 13 | | 15 | | 15 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 2 | | 2 | | 2 | | ns |
| Address Hold Time | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of Write | $t_{OW}$[1] | 2 | | 2 | | 2 | | 3 | | ns |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | | 7 | | 8 | | 9 | | 11 | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | |

*1. This parameter is guaranteed by design but not tested.*

### FIG. 4 AC TEST CIRCUIT

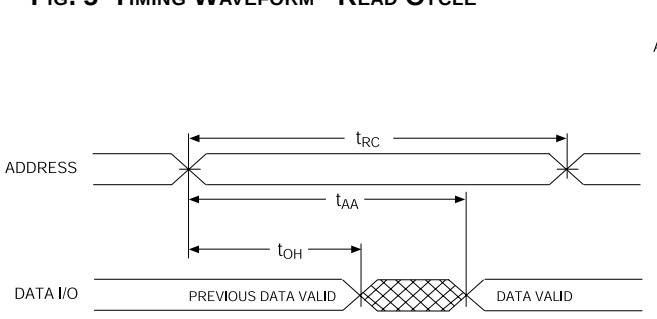



### AC TEST CONDITIONS

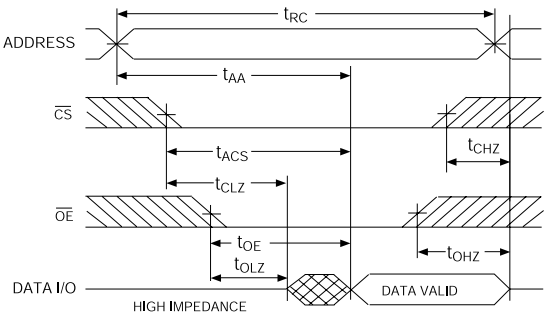
| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL} = 0, V_{IH} = 3.0$ | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

*Notes:*
*VZ is programmable from -2V to +7V.*
*IOL & IOH programmable from 0 to 16mA.*
*Tester Impedance Z0 = 75 Ω.*
*VZ is typically the midpoint of VOH and VOL.*
*IOL & IOH are adjusted to simulate a typical resistive load circuit.*
*ATE tester includes jig capacitance.*

## FIG. 5 TIMING WAVEFORM - READ CYCLE

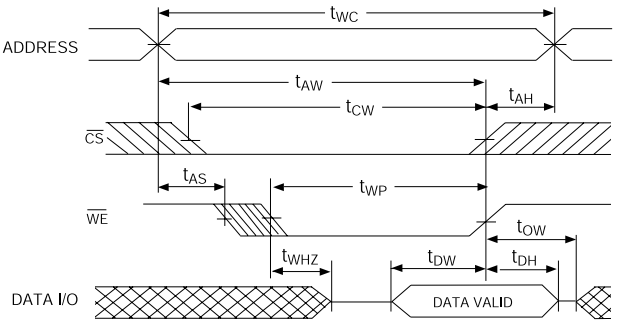



READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$)



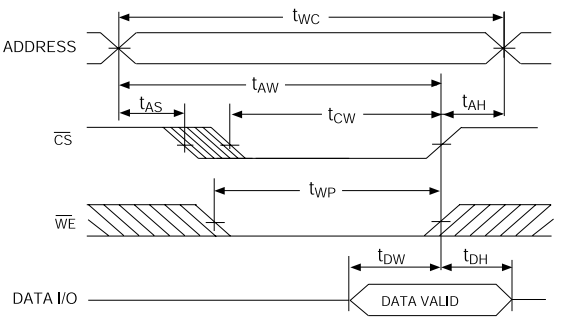

READ CYCLE 2 ($\overline{WE}$ = $V_{IH}$)

## FIG. 6 WRITE CYCLE - $\overline{WE}$ CONTROLLED



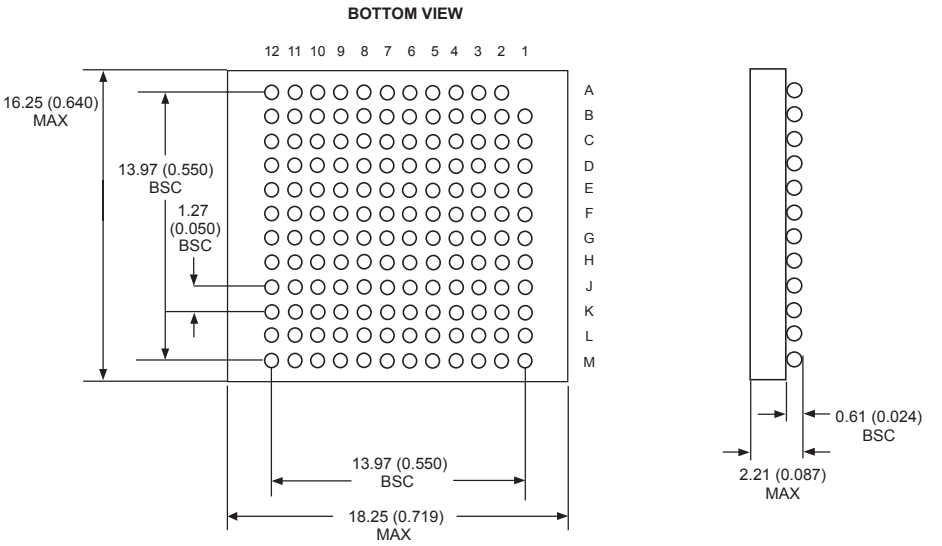

WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

## FIG. 6 WRITE CYCLE - $\overline{CS}$ CONTROLLED



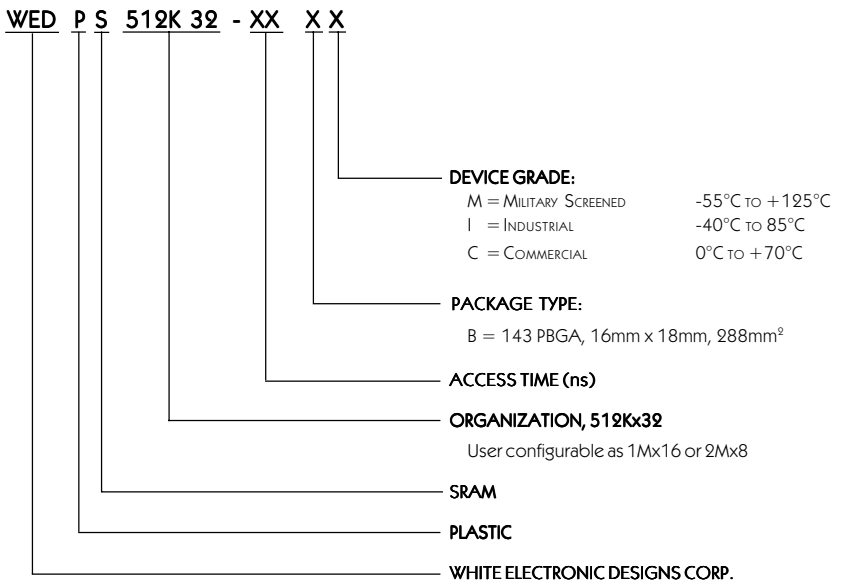

WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

## PACKAGE 756: 143 BALL GRID ARRAY




*ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES*

## ORDERING INFORMATION



## Document Title

512K x 32 SRAM Multi-Chip Package

## Revision History

| Rev # | History | ReleaseDate | Status |
|---|---|---|---|
| Rev 0 | Initial Release | March 6, 2002 | Advanced |
| Rev 1 | Switch Rows and Columns header position (Pg. 1) | March 13, 2002 | Advanced |
| Rev 2 | Switch Rows and Columns header position (Pg. 1) | May 6, 2002 | Advanced |
| Rev 3 | Change mechanical outline to more accurate design (Pg. 1,5) | May 14, 2002 | Advanced |
| Rev 4 | Remove references to 25-55ns speed grades (Pg. 1, 2, 3) | | Advanced |