



512Kx64 5V FLASH MODULE PRELIMINARY*

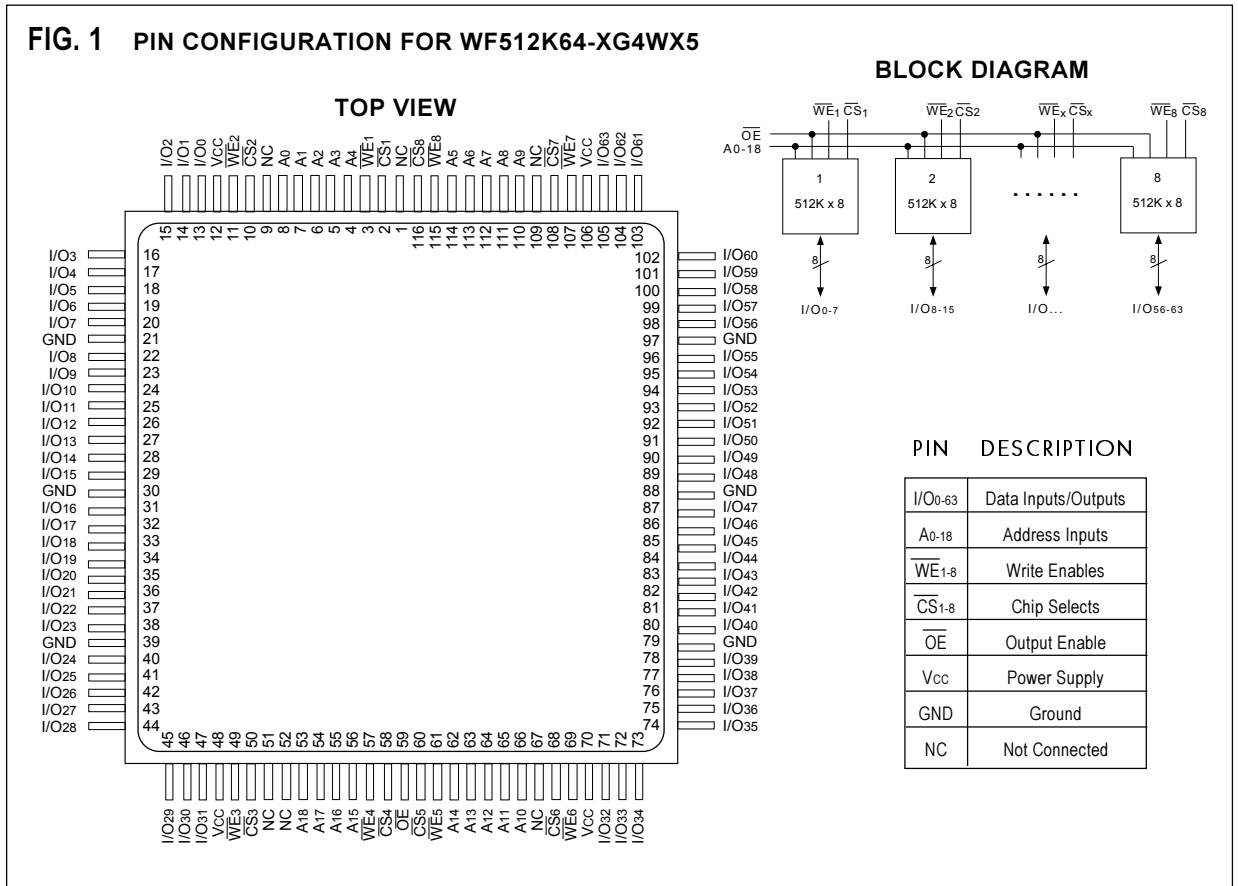
FEATURES

- Access Times of 70, 90, 120, 150ns
- Packaging
 - 116 lead, 40mm square, Hermetic CQFP (Package 504)
- 100,000 Erase/Program Cycles Minimum
- Sector Architecture
 - 8 equal size sectors of 64KBytes each
 - Any combination of sectors can be concurrently erased.
 - Also supports full chip erase
- Organized as 512Kx64, user configurable as 1Mx32, 2Mx16, or 4Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS, 6.5mA Standby
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time
- Weight
 - WF512K64-XG4WX5 - 20 grams typical

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WF512K64-XG4WX5





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V _{CC})	-2.0 to +7.0	V
Signal voltage range (any pin except A ₉) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention (Mil Temp)	20 years	
Endurance (write/erase cycles) (Mil Temp)	100,000 cycles min.	
A ₉ Voltage for sector protect (V _{ID}) (3)	-2.0 to +14.0	V

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A₉ pin is -0.5V. During voltage transitions, A₉ may overshoot V_{SS} to -2V for periods of up to 20ns. Maximum DC input voltage on A₉ is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	100	pF
WE capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CS capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	100	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C
A ₉ Voltage for Sector Protect	V _{ID}	11.5	12.5	V

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	µA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	µA
V _{CC} Active Current for Read (1)	I _{CC1}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz		380	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH}		480	mA
V _{CC} Standby Current	I _{CC4}	V _{CC} = 5.5, CS = V _{IH} , f = 5MHz		13	mA
V _{CC} Static Current	I _{CC3}	V _{CC} = 5.5, CS = V _{IH}		1.2	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{CS} CONTROLLED

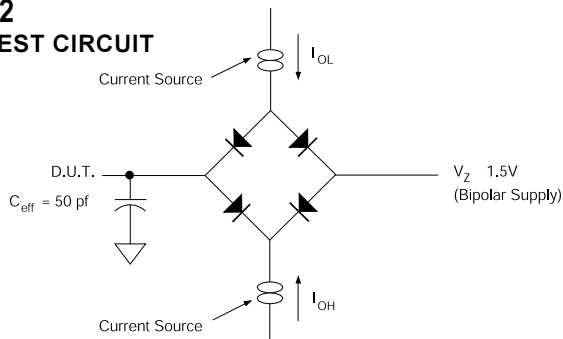
($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		90		120		150		ns
Write Enable Setup Time	tWLEL	tWS	0		0		0		0		ns
Chip Select Pulse Width	tELEH	tCP	45		45		50		50		ns
Address Setup Time	tAVEL	tAS	0		0		0		0		ns
Data Setup Time	tDVEH	tDS	45		45		50		50		ns
Data Hold Time	tEHDX	tDH	0		0		0		0		ns
Address Hold Time	tELAX	tAH	45		45		50		50		ns
Chip Select Pulse Width High	tEHEL	tCPH	20		20		20		20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300		300		300		300	μ s
Chip and Sector Erase Time (2)	tWHWH2			15		15		15		15	sec
Read Recovery Time	tGHLEL		0		0		0		0		ns
Chip Programming Time				11		11		11		11	sec
Chip Erase Time (3)				64		64		64		64	sec

NOTES:

1. Typical value for tWHWH1 is 7 μ s.
2. Typical value for tWHWH1 is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{WE} CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		90		120		150		ns
Chip Select Setup Time	tELWL	tCS	0		0		0		0		ns
Write Enable Pulse Width	tWLWH	tWP	45		45		50		50		ns
Address Setup Time	tAVWH	tAS	0		0		0		0		ns
Data Setup Time	tdVWH	tdS	45		45		50		50		ns
Data Hold Time	tWHDX	tdH	0		0		0		0		ns
Address Hold Time	tWHAX	tAH	45		45		50		50		ns
Write Enable Pulse Width High	tWHWL	tWPH	20		20		20		20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300		300		300		300	μs
Sector Erase Time (2)	tWHWH2			15		15		15		15	sec
Read Recovery Time before Write	tGHWL		0		0		0		0		ns
Vcc Set-up Time		tVCS	50		50		50		50		μs
Chip Programming Time				11		11		11		11	sec
Output Enable Setup Time		tOES	0		0		0		0		ns
Output Enable Hold Time (4)		tOEH	10		10		10		10		ns
Chip Erase Time (3)				64		64		64		64	sec

NOTES:

1. Typical value for tWHWH1 is 7μs.
2. Typical value for tWHWH1 is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	70		90		120		150		ns
Address Access Time	tAVQV	tACC		70		90		120		150	ns
Chip Select Access Time	tELQV	tCE		70		90		120		150	ns
Output Enable to Output Valid	tGLQV	tOE		35		35		50		55	ns
Chip Select to Output High Z (1)	tEHQZ	tDF		20		20		30		35	ns
Output Enable High to Output High Z (1)	tGHQZ	tDF		20		20		30		35	ns
Output Hold from Address, \overline{CS} or \overline{OE} Change, whichever is First	tAXQX	tOH	0		0		0		0		ns

1. Guaranteed by design, but not tested



FIG. 3
AC WAVEFORMS FOR READ OPERATIONS

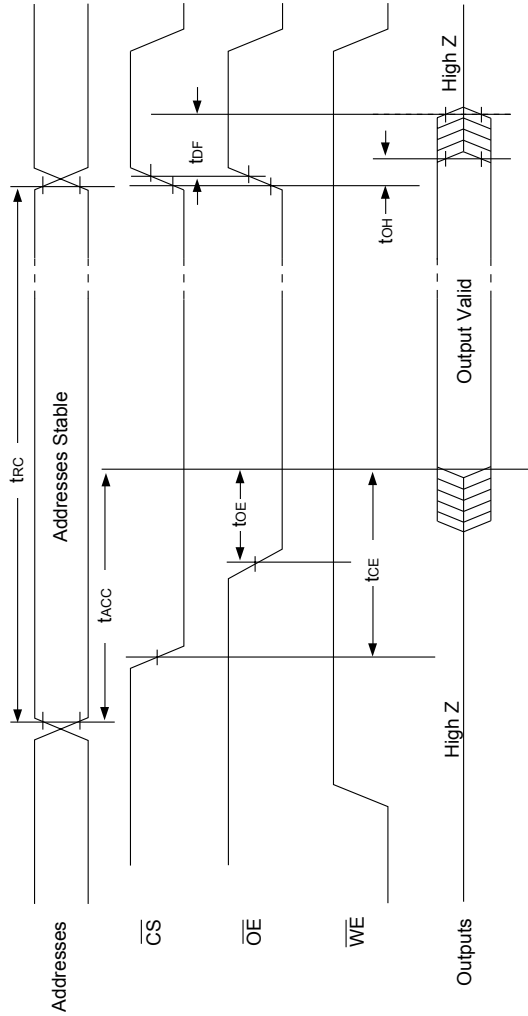
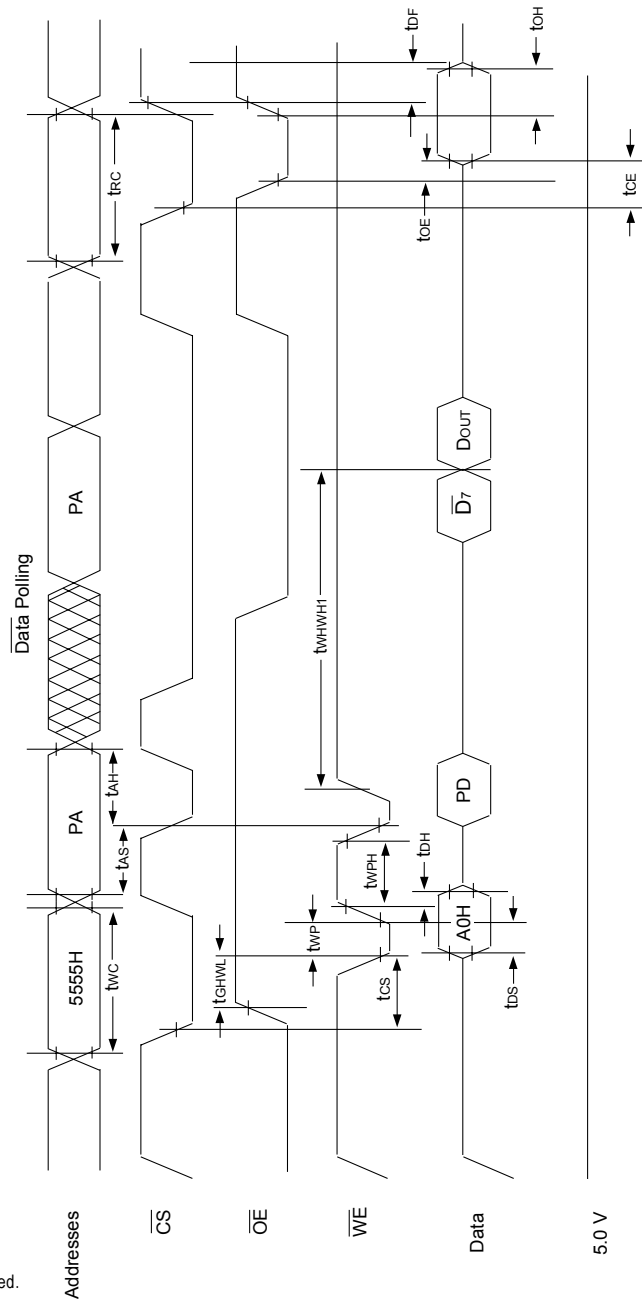




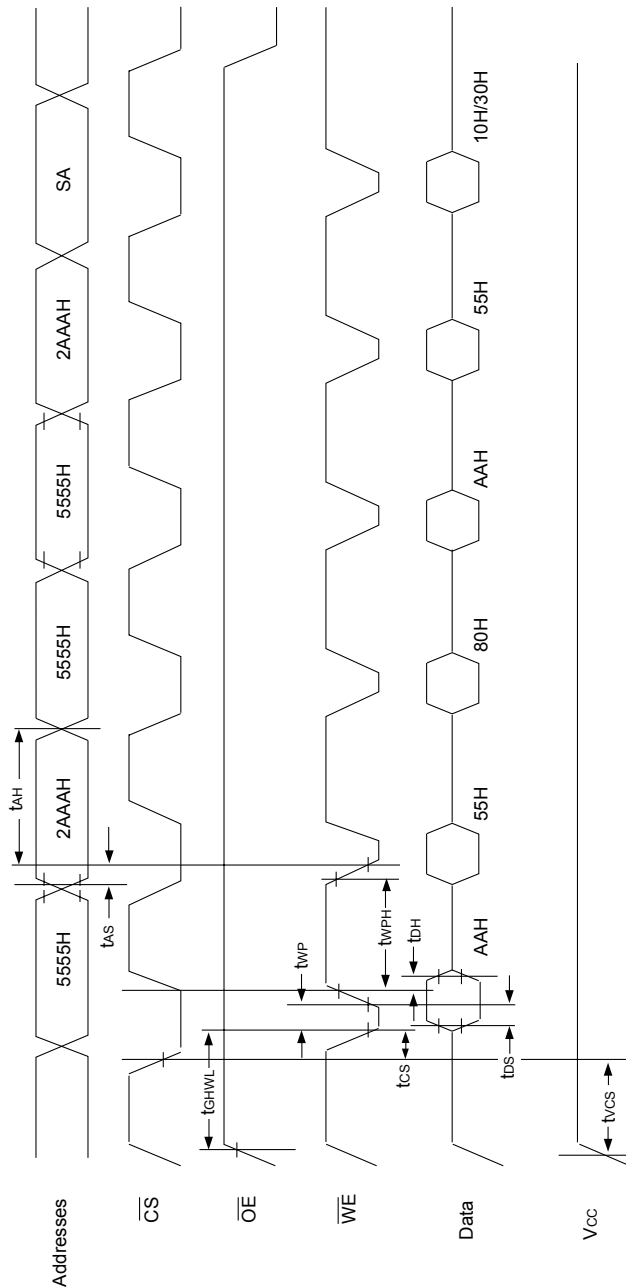
FIG. 4
WRITE/ERASE/PROGRAM
OPERATION, WE CONTROLLED



- NOTES:**
1. PA is the address of the memory location to be programmed.
 2. PD is the data to be programmed at byte address.
 3. $\overline{D7}$ is the output of the complement of the data written to each chip.
 4. Dout is the output of the data written to the device.
 5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 5
AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.



FIG. 6
AC WAVEFORMS FOR DATA POLLING
DURING EMBEDDED ALGORITHM OPERATIONS

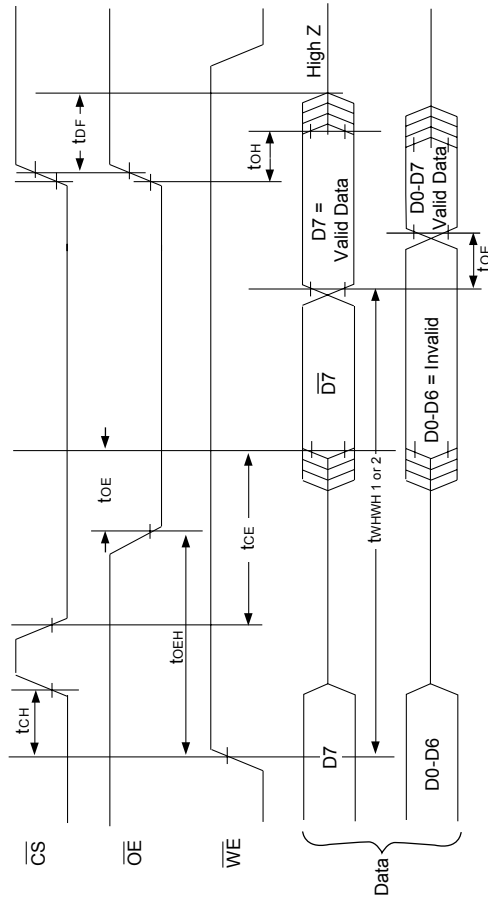
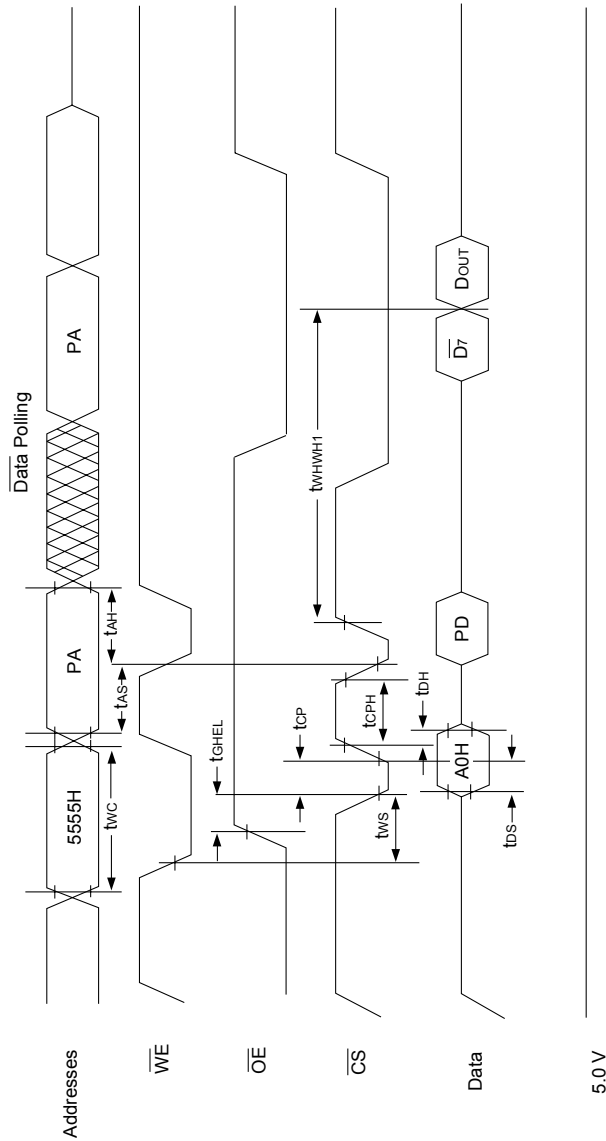




FIG. 7
ALTERNATE \overline{CS} CONTROLLED
PROGRAMMING OPERATION TIMINGS

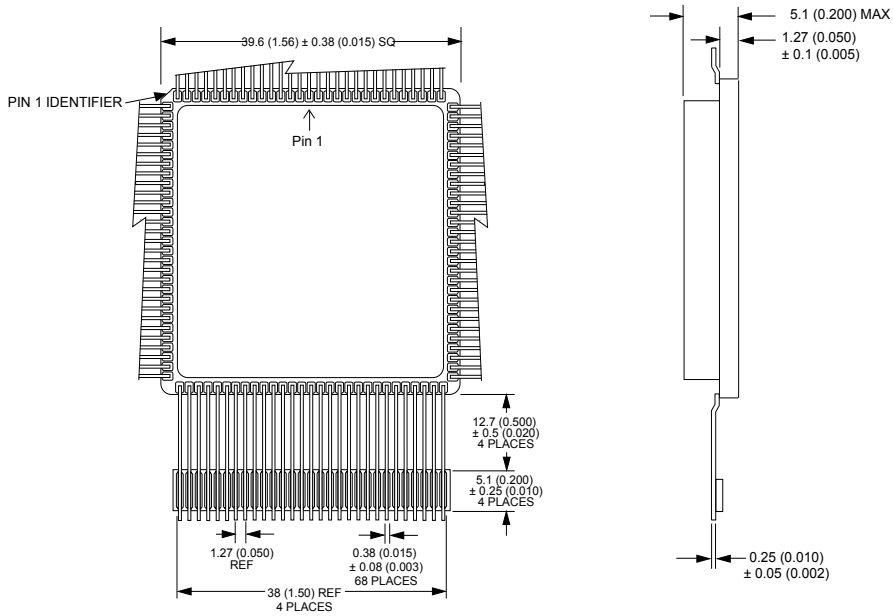


Notes:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to each chip.
4. Dout is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



PACKAGE 504: 116 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4W)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 512K64 - XXX G4W X 5

