



# 512Kx32 SRAM / FLASH MODULE

PRELIMINARY\*

## FEATURES

- Access Times of 25ns (SRAM) and 70, 90ns (FLASH)
- Packaging
  - 66 pin, PGA Type, 1.385" square HIP, Hermetic Ceramic HIP (Package 402)
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880") square (Package 509) 4.57mm (0.180") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2). Package to be developed.
- 512Kx32 SRAM
- 512Kx32 5V Flash
- Organized as 512Kx32 of SRAM and 512Kx32 of Flash Memory with common Data Bus
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs

- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

## FLASH MEMORY FEATURES

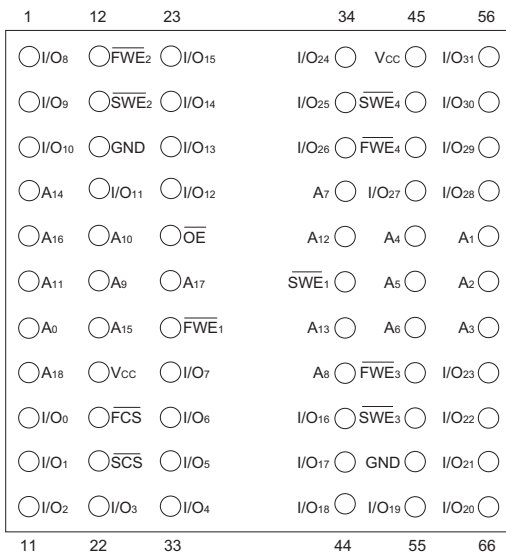
- 100,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 64KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

\* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

Note: Programming information available upon request.

FIG. 1 PIN CONFIGURATION FOR WSF512K32-29H2X

TOP VIEW



## PIN DESCRIPTION

I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-18</sub>	Address Inputs
$\overline{\text{SWE}}_{1-4}$	SRAM Write Enables
$\overline{\text{SCS}}$	SRAM Chip Select
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground
NC	Not Connected
$\overline{\text{FWE}}_{1-4}$	Flash Write Enables
$\overline{\text{FCS}}$	Flash Chip Select

## BLOCK DIAGRAM

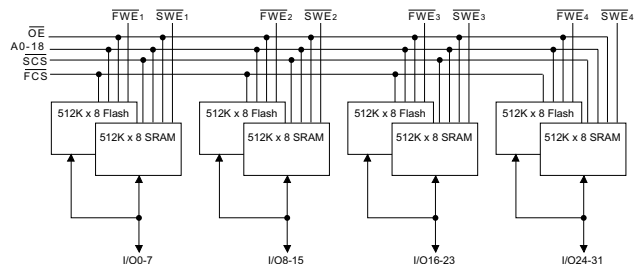
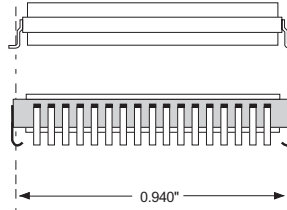
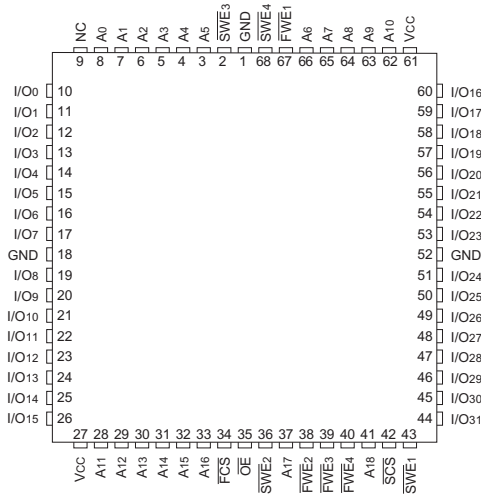




FIG. 2 PIN CONFIGURATION FOR WSF512K32-29G2TX

TOP VIEW

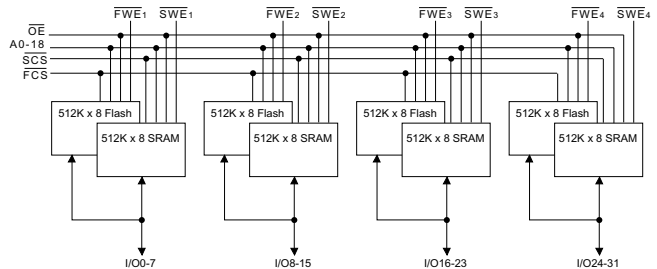


The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
SWE1-4	SRAM Write Enables
SCS	SRAM Chip Select
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected
FWE1-4	Flash Write Enables
FCS	Flash Chip Select

BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	7.0	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

Parameter	
Flash Data Retention	20 years
Flash Endurance (write/erase cycles)	100,000

### NOTE:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V

## SRAM TRUTH TABLE

$\overline{SCS}$	$\overline{OE}$	$\overline{SWE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

### NOTE:

1.  $\overline{FCS}$  must remain high when  $\overline{SCS}$  is low.

## CAPACITANCE (T<sub>A</sub> = +25°C)

Test	Symbol	Condition	Max	Unit
$\overline{OE}$ Capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	80	pF
F/S WE <sub>1-4</sub> Capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	30	pF
F/S $\overline{CS}$ Capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	50	pF
D <sub>0-31</sub> Capacitance	C <sub>I/O</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	30	pF
A <sub>0-18</sub> Capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	80	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS (V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{SCS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
SRAM Operating Supply Current x 32 Mode	I <sub>CCx32</sub>	$\overline{SCS}$ = V <sub>IL</sub> , $\overline{OE}$ = $\overline{FCS}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		550	mA
Standby Current	I <sub>SB</sub>	$\overline{FCS}$ = $\overline{SCS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		90	mA
SRAM Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4	V
SRAM Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		V
Flash V <sub>CC</sub> Active Current for Read (1)	I <sub>CC1</sub>	$\overline{FCS}$ = V <sub>IL</sub> , $\overline{OE}$ = $\overline{SCS}$ = V <sub>IH</sub>		250	mA
Flash V <sub>CC</sub> Active Current for Program or Erase (2)	I <sub>CC2</sub>	$\overline{FCS}$ = V <sub>IL</sub> , $\overline{OE}$ = $\overline{SCS}$ = V <sub>IH</sub>		300	mA
Flash Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12.0mA, V <sub>CC</sub> = 4.5		0.45	V
Flash Output High Voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5	0.85 x V <sub>CC</sub>		V
Flash Output High Voltage	V <sub>OH2</sub>	I <sub>OH</sub> = -100 μA, V <sub>CC</sub> = 4.5	V <sub>CC</sub> - 0.4		V
Flash Low V <sub>CC</sub> Lock Out Voltage	V <sub>LKO</sub>		3.2	4.2	V

### NOTES:

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with  $\overline{OE}$  at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**SRAM AC CHARACTERISTICS**  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol	-25		Unit
		Min	Max	
Read Cycle				
Read Cycle Time	t <sub>RC</sub>	25		ns
Address Access Time	t <sub>AA</sub>		25	ns
Output Hold from Address Change	t <sub>OH</sub>	0		ns
Chip Select Access Time	t <sub>ACS</sub>		25	ns
Output Enable to Output Valid	t <sub>OE</sub>		15	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	3		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		12	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		12	ns

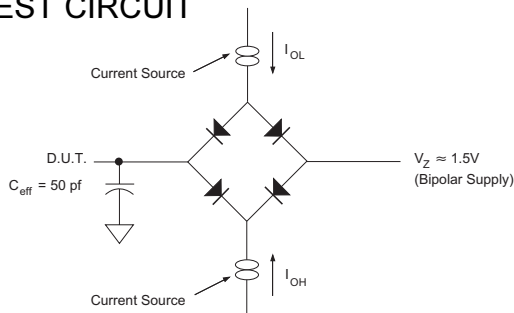
1. This parameter is guaranteed by design but not tested.

**SRAM AC CHARACTERISTICS**  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol	-25		Unit
		Min	Max	
Write Cycle				
Write Cycle Time	t <sub>WC</sub>	25		ns
Chip Select to End of Write	t <sub>CW</sub>	20		ns
Address Valid to End of Write	t <sub>AW</sub>	20		ns
Data Valid to End of Write	t <sub>DW</sub>	15		ns
Write Pulse Width	t <sub>WP</sub>	20		ns
Address Setup Time	t <sub>AS</sub>	3		ns
Address Hold Time	t <sub>AH</sub>	0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	3		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		15	ns
Data Hold from Write Time	t <sub>DH</sub>	0		ns

1. This parameter is guaranteed by design but not tested.

**FIG. 3**  
**AC TEST CIRCUIT**



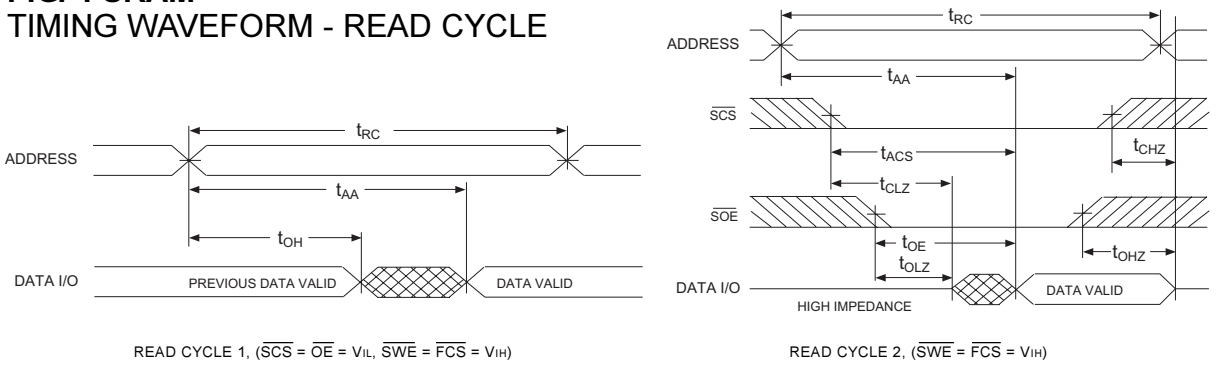
**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

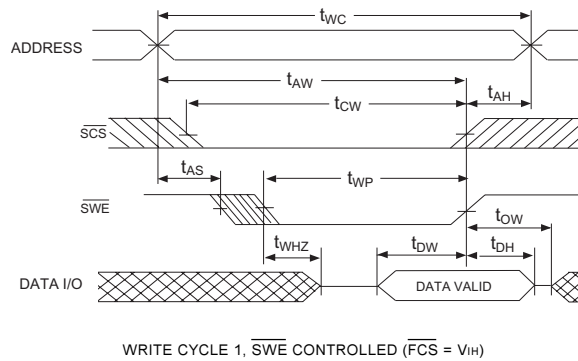
**NOTES:**  
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



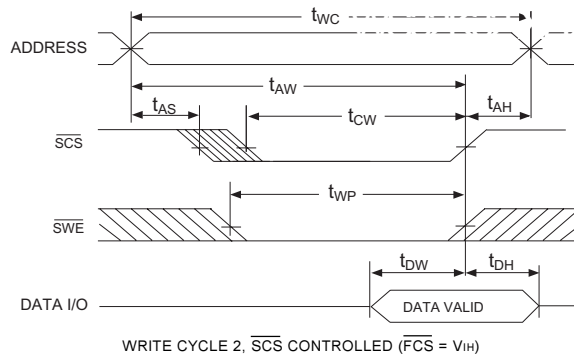
**FIG. 4 SRAM**  
TIMING WAVEFORM - READ CYCLE



**FIG. 5 SRAM**  
WRITE CYCLE -  $\overline{SWE}$  CONTROLLED



**FIG. 6 SRAM**  
WRITE CYCLE -  $\overline{SCS}$  CONTROLLED





**FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FWE CONTROLLED**  
**(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)**

Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	70		90		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	45		45		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	45		45		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		ns
Address Hold Time	t <sub>WLAX</sub>	t <sub>AH</sub>	45		45		ns
Write Enable Pulse Width High	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300		300	µs
Chip and Sector Erase Time (2)	t <sub>WHWH2</sub>			15		15	sec
Read Recovery Time Before Write	t <sub>GHWL</sub>		0		0		µs
V <sub>CC</sub> Set-up Time		t <sub>VCS</sub>	50		50		µs
Chip Programming Time				11		11	sec
Output Enable Setup Time		t <sub>OES</sub>	0		0		ns
Output Enable Hold Time (4)		t <sub>OEH</sub>	10		10		ns
Chip Erase Time (3)				64		64	sec

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7ns.
2. Typical value for t<sub>WHWH2</sub> is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data Polling.

**FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS**  
**(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)**

Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	70		90		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>ACC</sub>		70		90	ns
Chip Select Access Time	t <sub>ELQV</sub>	t <sub>CE</sub>		70		90	ns
OE to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		35		35	ns
Chip Select to Output High Z (1)	t <sub>EHQZ</sub>	t <sub>DF</sub>		20		20	ns
OE High to Output High Z (1)	t <sub>GHQZ</sub>	t <sub>DF</sub>		20		20	ns
Output Hold from Address, FCS or OE Change, whichever is first	t <sub>AXQX</sub>	t <sub>OH</sub>	0		0		ns

1. Guaranteed by design, not tested.



FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, FCS CONTROLLED  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)

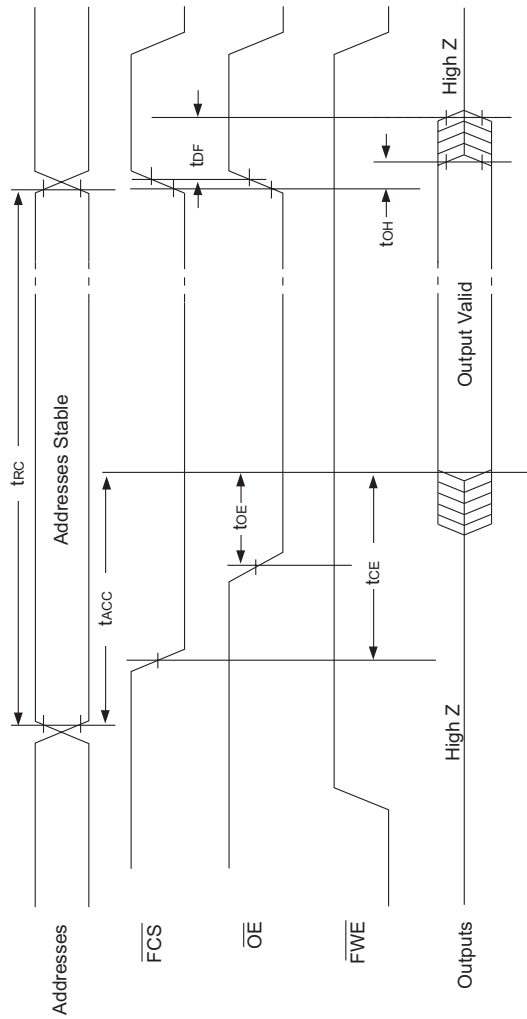
Parameter	Symbol		-70		-90		Unit
			Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		90		ns
FWE Setup Time	tWLEL	tWS	0		0		ns
FCS Pulse Width	tELEH	tCP	45		45		ns
Address Setup Time	tAVEL	tAS	0		0		ns
Data Setup Time	tDVEH	tDS	45		45		ns
Data Hold Time	tEHDX	tDH	0		0		ns
Address Hold Time	tELAX	tAH	45		45		ns
FCS Pulse Width High	tEHEL	tCPH	20		20		ns
Duration of Programming Operation (1)	tWHWH1			300		300	µs
Sector Erase Time (2)	tWHWH2			15		15	sec
Read Recovery Time	tGHEL		0		0		ns
Chip Programming Time				11			sec
Chip Erase Time (3)				64			sec

NOTES:

1. Typical value for tWHWH1 is 7ns.
2. Typical value for tWHWH2 is 1sec.
3. Typical value for Chip Erase Time is 8sec.



**FIG. 7**  
AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS

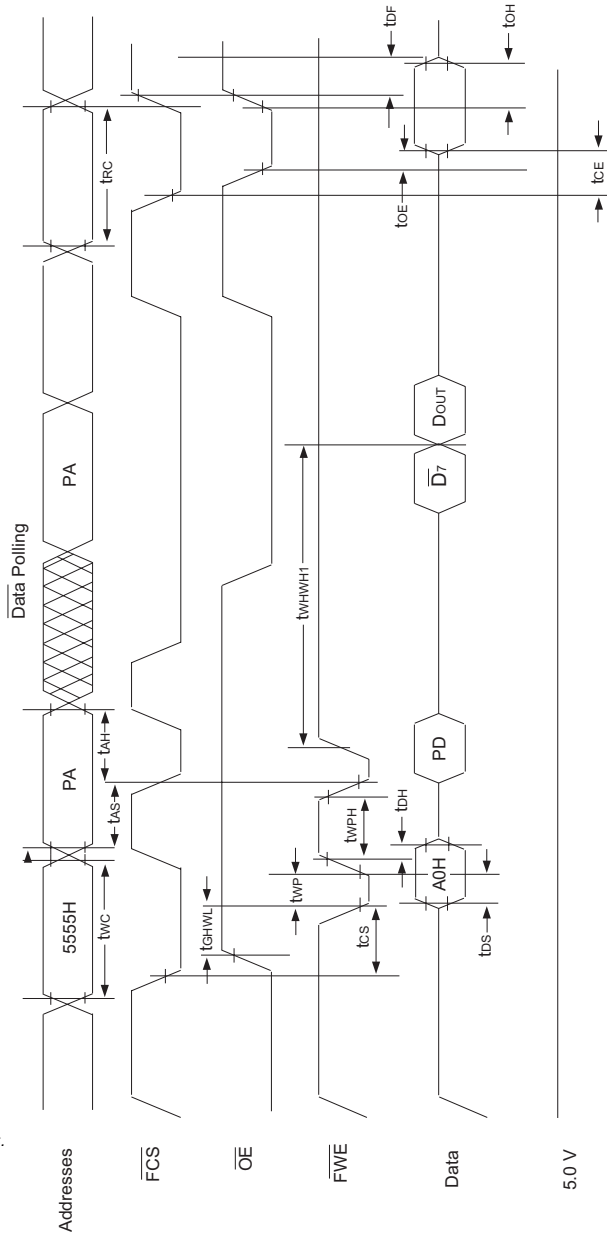


**Note:**  $\overline{Scs} = V_{IH}$





FIG. 8  
WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY FWE CONTROLLED

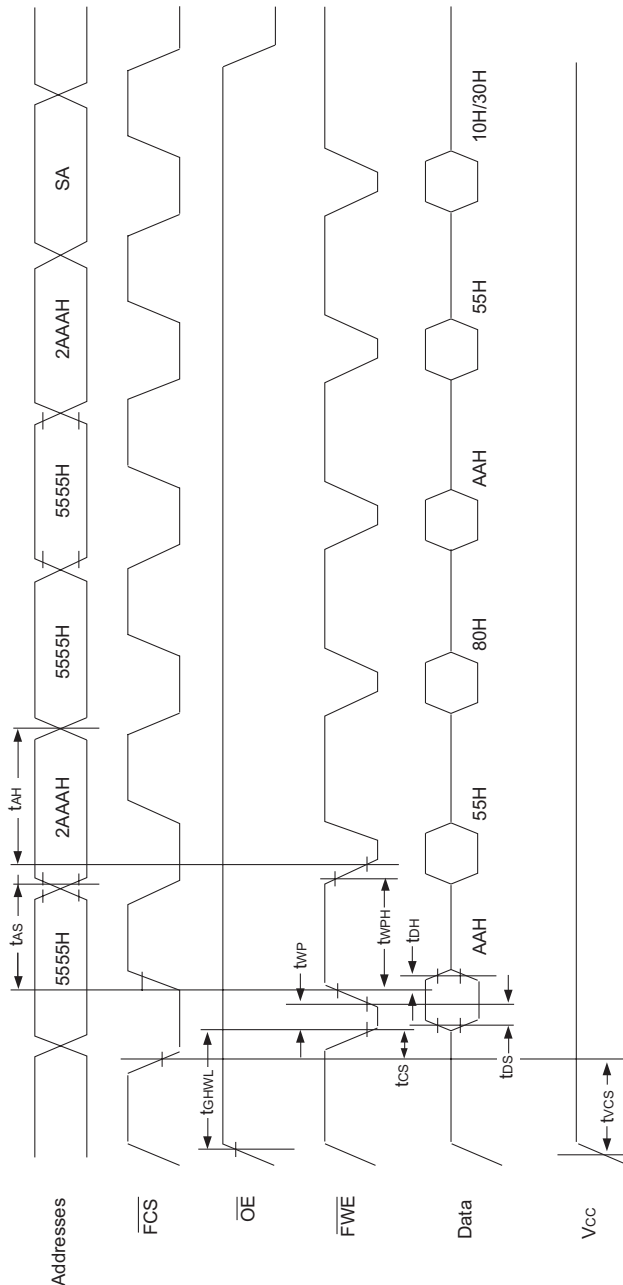


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.
6. SCS =  $V_{IH}$



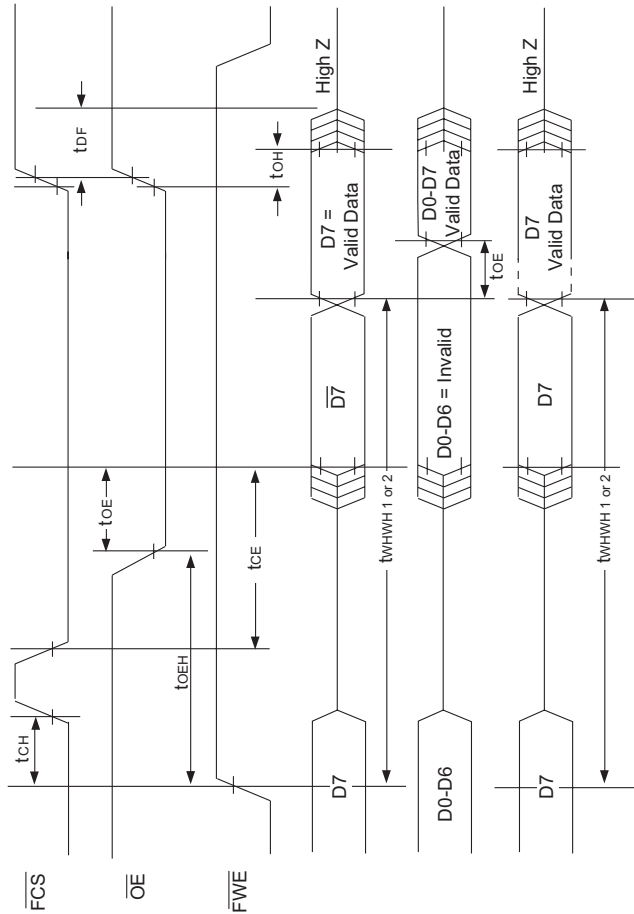
FIG. 9  
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



- Notes:
1. SA is the sector address for Sector Erase.
  2.  $\overline{SCS} = V_{IH}$



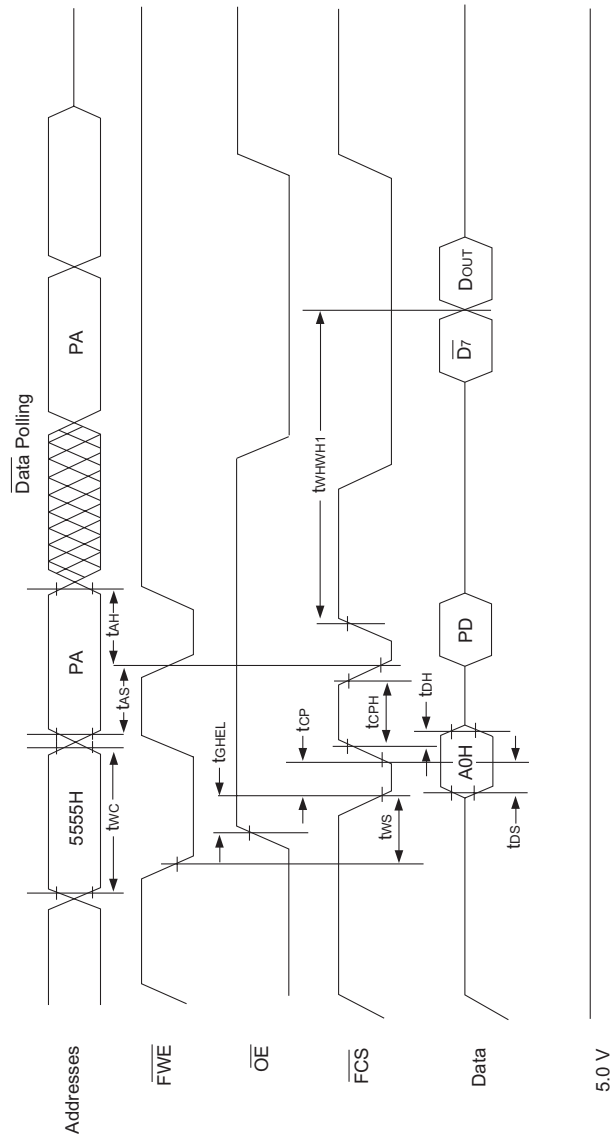
FIG. 10 AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY



Note:  $\overline{SCS} = V_{IH}$



FIG. 11  
WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY,  $\overline{CS}$  CONTROLLED

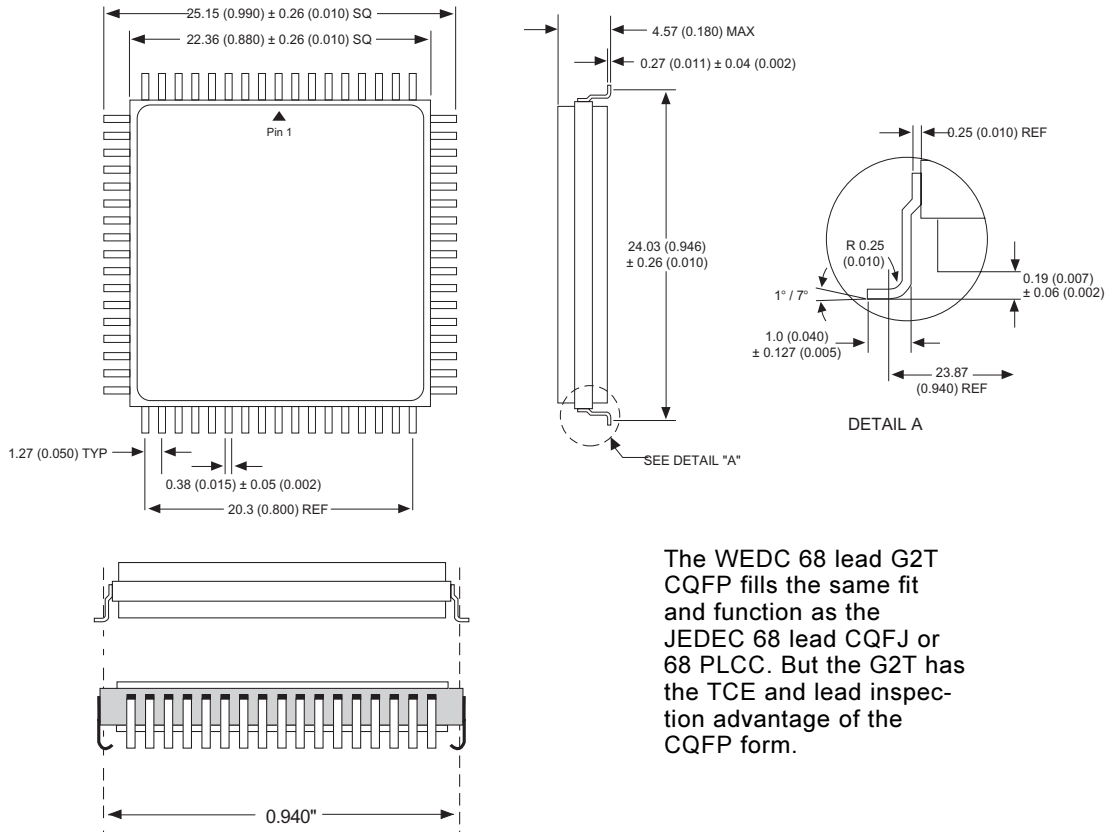


NOTES:

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4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.
6.  $\overline{SCS} = V_{IH}$



**PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)**

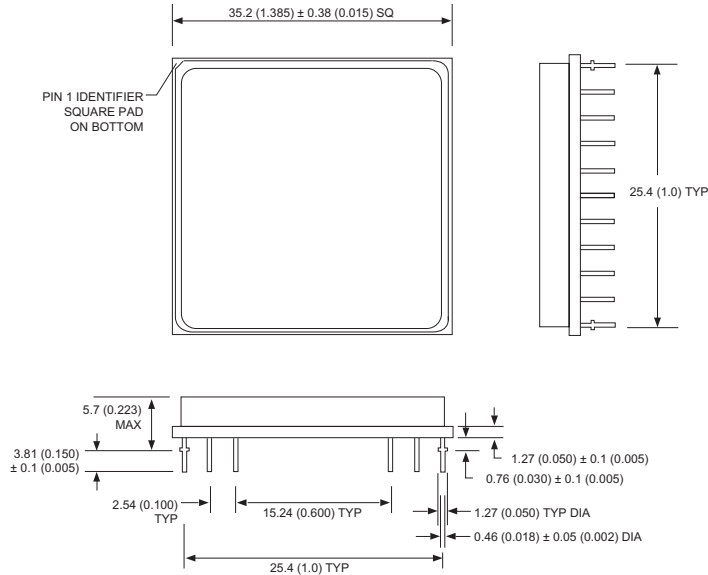


The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WSF 512K32 - 29 XXX

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H2 = Ceramic Hex In-line Package, HIP (Package 402)
- G2T = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 509)

ACCESS TIME (ns)

- 29 = 25ns SRAM and 90ns FLASH

ORGANIZATION, 512K x 32 SRAM and Flash

Flash

SRAM

WHITE ELECTRONIC DESIGNS CORP.