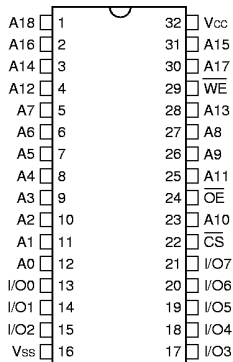




512Kx8 SRAM

PRELIMINARY *

PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
Vss	Ground

PLASTIC PLUS™ FEATURES

- Access Times 55, 70, 85ns
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard Packages:
 - 32 Pin 600mil Plastic DIP
 - 32 Lead 525mil Plastic SOP
 - 32 Lead 400mil Plastic TSOP (II)
- Electrical and Speed Characteristics for:
 - Military Temperature (-55°C to +125°C)
 - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Organized as 512K x 8
- 5 Volt Power Supply
- Low Power CMOS
- Battery Back-Up Operation
- Reliability Test Data Available:
 - High Temperature Operating Life
 - High Temperature Storage
 - Pressure Cooker Test
 - Wet High Temperature Operating Life
 - Thermal Shock
 - Temperature Cycling

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

PLASTIC PLUS SRAM

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T _A	-55	+125	°C
Operating Temperature (Ind.)	T _A	-40	+85	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to V _{SS}	V _G	-0.5	V _{CC} + 0.5	V
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T _A	-55	+125	°C
Operating Temperature (Ind.)	T _A	-40	+85	°C

TRUTH TABLE

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O Pin	V _{CC} Current
H	X	X	Power Down	High-Z	I _{SB}
L	H	H	Out Disable	High-Z	I _{CC}
L	H	L	Read	D _{OUT}	I _{CC}
L	L	X	Write	D _{IN}	I _{CC}

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	8	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	10	pF

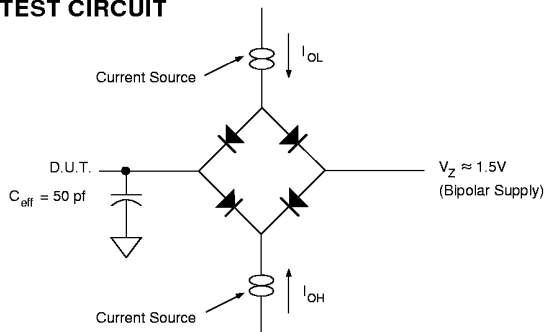
This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min		Max		Units
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = V _{SS} to V _{CC}			10		μA
Output Leakage Current	I _{LO}	$\overline{CS} = V_{IH}, \overline{OE} = V_{IH}, V_{OUT} = V_{SS}$ to V _{CC}			10		μA
Operating Supply Current	I _{CC}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$			85		mA
Standby Current	I _{SB}	$\overline{CS} = V_{CC}, \overline{OE} = V_{IH}, f = 5\text{MHz}$			8		mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5			0.4		V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4				V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V**DATA RETENTION CHARACTERISTICS**(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min			Typ			Max			Units
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - .2V$	2.0						5.5			V
Data Retention Current	I _{CCDR}	V _{CC} = 3V				10			150			μA

AC TEST CIRCUIT**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



AC CHARACTERISTICS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-55		-70		-85		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	55		70		85		ns
Address Access Time	t _{AA}		55		70		85	ns
Output Hold from Address Change	t _{OH}	5		5		5		ns
Chip Select Access Time	t _{ACS}		55		70		85	ns
Output Enable to Output Valid	t _{OE}		25		35		45	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	10		10		10		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	5		5		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		20		25		30	ns
Output Disable to Output in High Z	t _{OHZ} ¹		20		25		30	ns

1. This parameter is guaranteed by design but not tested.

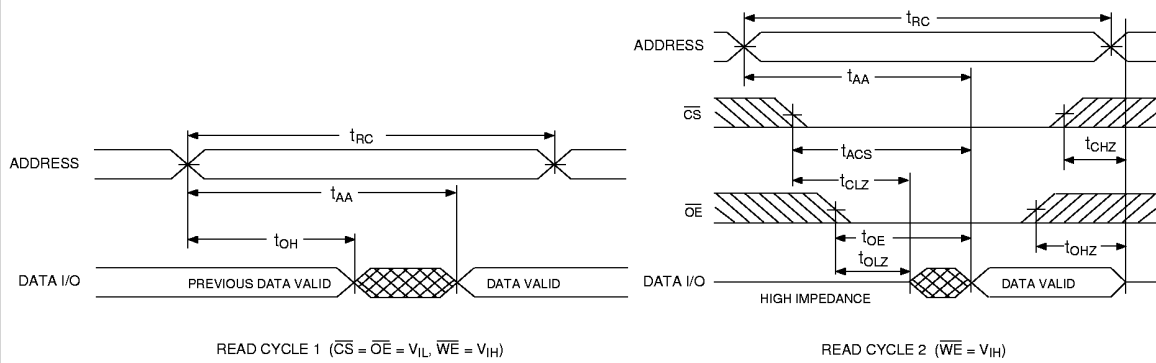
AC CHARACTERISTICS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-55		-70		-85		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	55		70		85		ns
Chip Select to End of Write	t _{CW}	45		60		70		ns
Address Valid to End of Write	t _{AW}	45		60		70		ns
Data Valid to End of Write	t _{DW}	25		30		35		ns
Write Pulse Width	t _{WP}	40		50		55		ns
Address Setup Time	t _{AS}	0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	5		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		25		30		35	ns
Data Hold Time	t _{DH}	0		0		0		ns

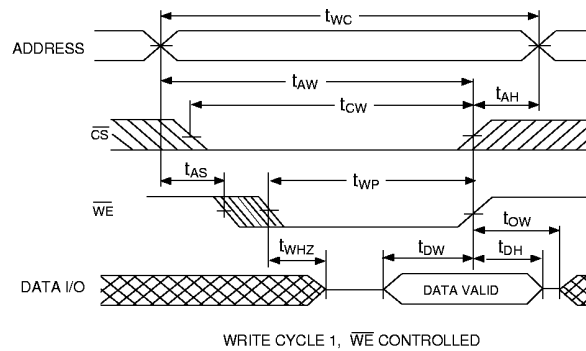
1. This parameter is guaranteed by design but not tested.



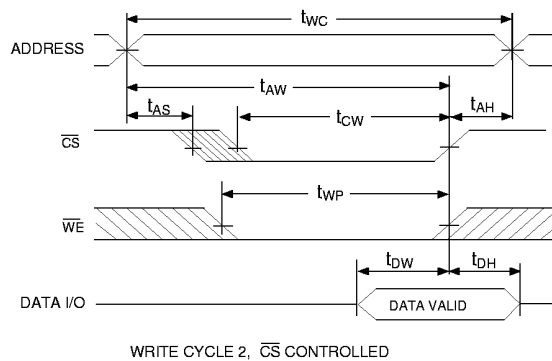
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED

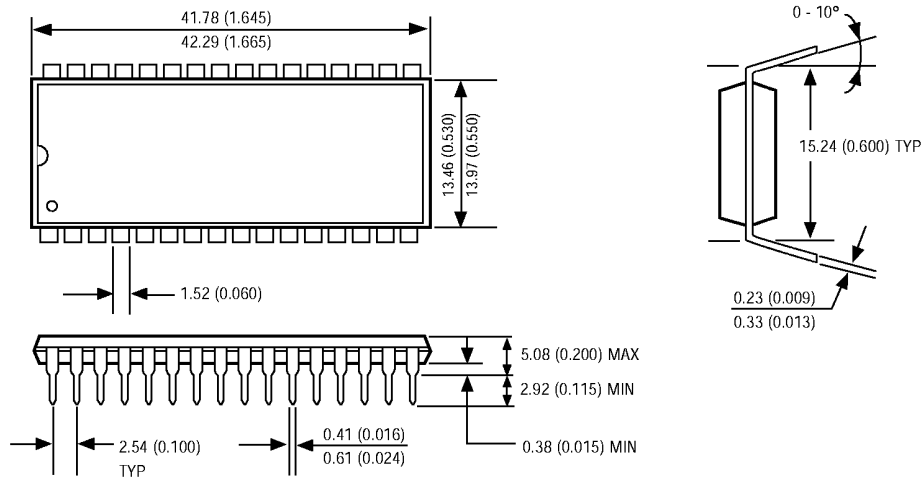


WRITE CYCLE - \overline{CS} CONTROLLED



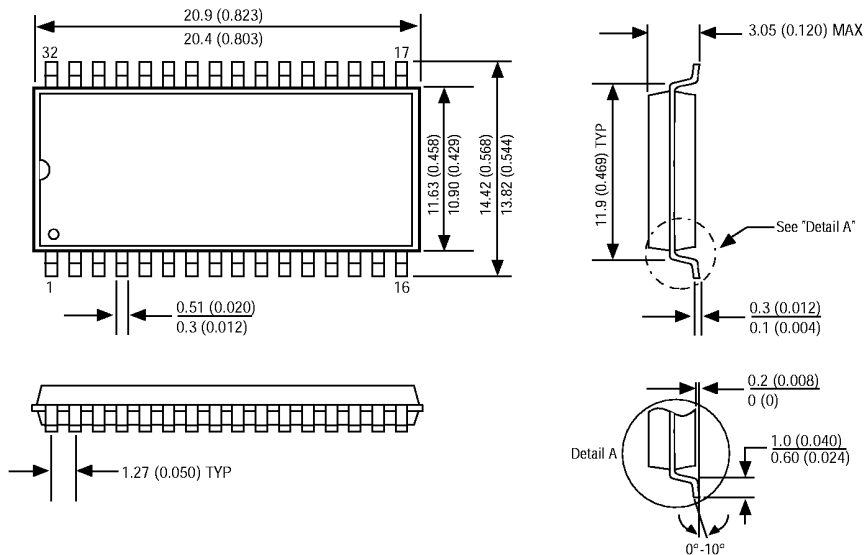


32 PIN, PLASTIC DIP PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

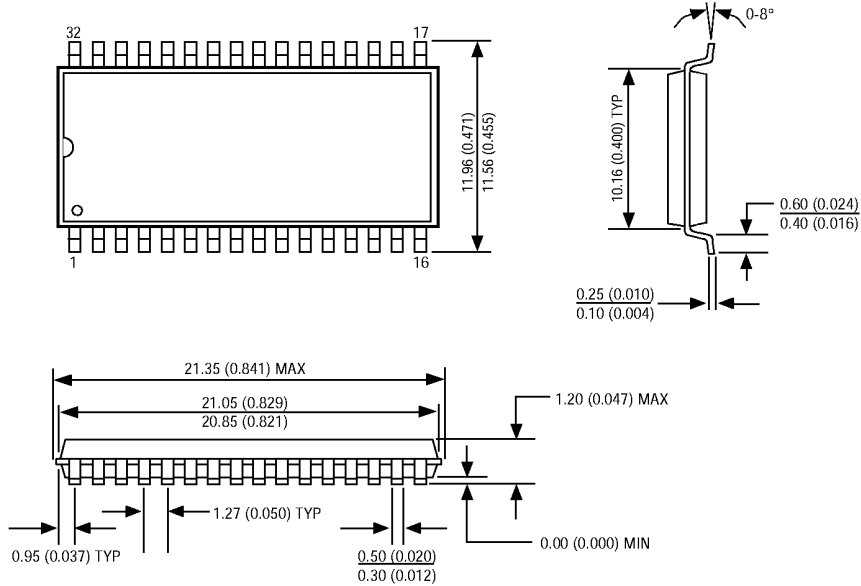
32 LEAD, PLASTIC SOP PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

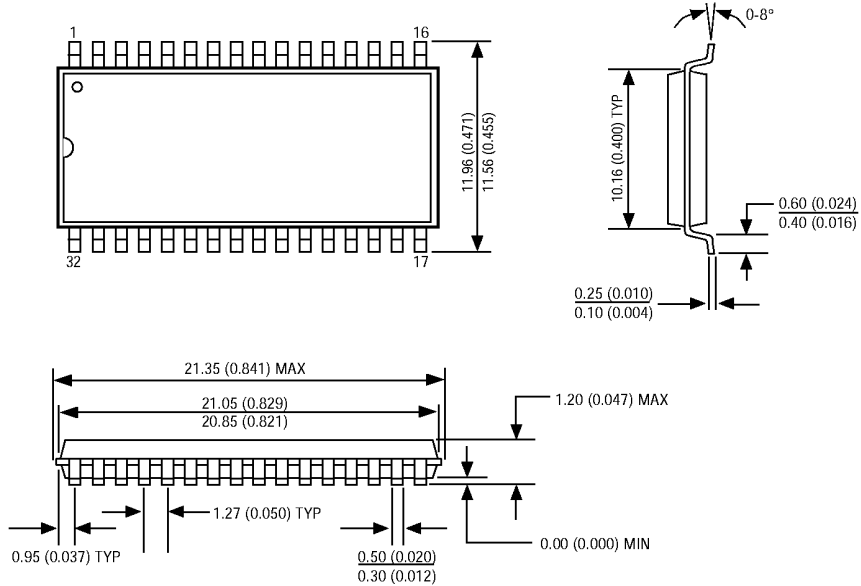


32 LEAD, PLASTIC TSOP (II) FORWARD PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, PLASTIC TSOP (II) REVERSE PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)



ORDERING INFORMATION

W P S 512K 8 L X - XXX X X

DEVICE GRADE:

- M = Military Temperature -55°C to +125°C
- I = Industrial Temperature -40°C to +85°C

PACKAGE:

- W = 32 pin 600mil Plastic DIP
- G = 32 lead 525mil SOP
- T = 32 lead 400mil TSOP (II) Forward
- R = 32 lead 400mil TSOP (II) Reverse

ACCESS TIME (ns)

IMPROVEMENT MARK

- B = Burn-in
- T = Temperature Cycling
- C = Burn-in and Temperature Cycle
- L = Low Power

ORGANIZATION, 512K x 8

SRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS