The containing the primary functions required for DC to onverters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, drive and a high current output switch. This series was specifically designed to be incorporated in step-up, step-down and voltage-inverting applications with a minimum number of external components.

8 DIP 8 SOP

PIN:

1. Switch Collector
2. Switch Emitter
3. Timing Capacitor
4. GND
5. Comparator Inverting Input
6. VCC
7. IPK Sense
8. Driver Collector

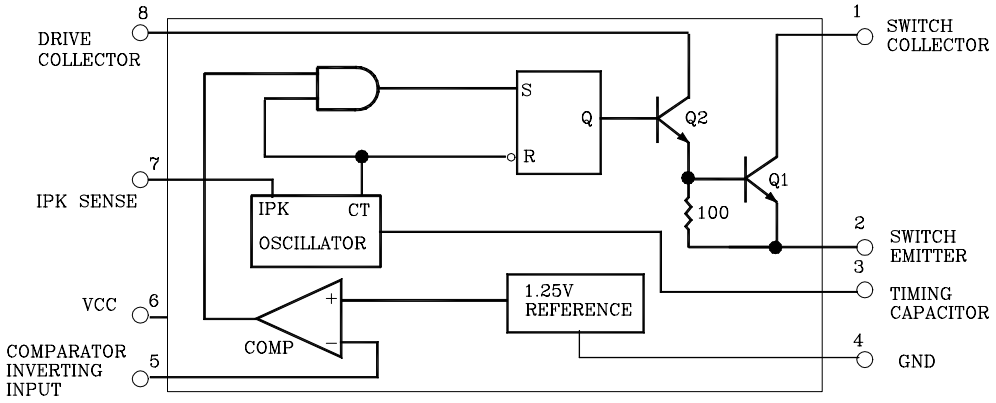
FEATURES

- Operation from 3 to 40V input
- Low standby current
- Current limiting
- Output switch current to 1.5A
- Precision 2% reference
- Output - voltage adjustable
- Frequency of operation from 100Hz to 100KHz

ORDERING INFORMATION

Device	Operating temperature	Package
34063	0 ~ +70℃	8 DIP
34063	0 ~ +70℃	8 SOP

BLOCK DIAGRAM



Wing Shing Computer Components Co., (H.K.)Ltd. Tel:(852)2341 9276 Fax:(852)2797 8153
Homepage: http://www.wingshing.com E-mail: wsccltd@hkstar.com

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	-0.3 ~ +40	Vdc
Switch Collector Voltage	$V_{C(SW)}$	40	Vdc
Switch Emitter Voltage	$V_{E(SW)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(SW)}$	40	Vdc
Driver Collector Voltage	$V_{C(drive)}$	40	Vdc
Drive Collector Current (Note 1)	$I_{C(drive)}$	100	mA
Switch Current	Isw	1.5	A
Operating Junction Temperature	T_J	+150	℃
Operating Ambient Temperature Range	T_A	0 to +70	℃
Storage Temperature Range	Tstg	-65 to +150	℃

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V. Ta= Tlow to Thigh. unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OSCILLATOR						
Frequency	fosc	V_{PIN5}=0V, C_T=1.0nF , T_A=25℃	24	33	42	KHz
Charging Current	I_{chg}	V_{CC}=5 to 40V, T_A=25℃	24	35	42	μA
Discharge Current	I_{dischg}	V_{CC}=5 to 40V, T_A=25℃	140	220	260	μA
Discharge To Charge Current Ratio	I_{dischg}/I_{chg}	Pin7 to V_{CC} , T_A=25℃	5.2	6.5	7.5	-
Current Limit Sense Voltage	$V_{IPK(sense)}$	I_{chg} = $I_{dischg,}$ T_A=25℃	250	300	350	mV
OUTPUT SWITCH(NOTE 2)						
Saturation Voltage , Darlington Connection	$V_{CE(sat)}$	Isw=1.0A, Pins1,8 connected	-	1.0	1.3	V
Saturation Voltage , Darlington Connection	$V_{CE(sat)}$	Isw=1.0A, R_{PIN8}=82Ω to Vcc, Forced β ≧20	-	0.45	0.7	V
DC Current Gain	h_{FE}	Isw=1.0A, V_{CE} = 5.0V, T_A=25℃	50	75	-	-
Collector Off- State Current	$I_{C(off)}$	V_{CE} =40V	-	40	100	μA
COMPARATOR						
Threshold Voltage	V_{TH}	T_A=25℃ T_A=Tlow to Thigh	1.225 1.21	1.25 -	1.275 1.29	V
Threshold Voltage Line Regulation	Regline	V_{CC} = 3 to 40V		1.4	5.0	mV
Input Bias Current	I_{IB}	V_{IN}=0V		-20	-400	nA
TOTAL DEVICE						
Supply Current	I_{CC}	V_{CC}=5 to 40V, C_T=1.0nF, Pin7=Vcc ,V_{PIN} 5>Vth Pin 2 =GND, remaining pins open	-	-	4.0	mA

Notes : 1.Maximum package power dissipation limits must be observed.

2.Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

FIGURE 1.OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

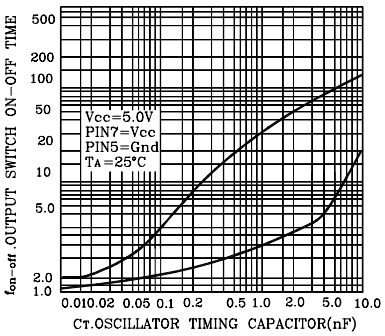


FIGURE 2.TIMING CAPACITOR WAVEFORM

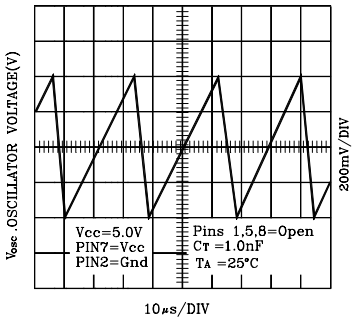


FIGURE 3.EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

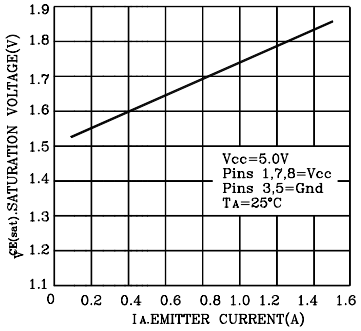


FIGURE 4.COMMON EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

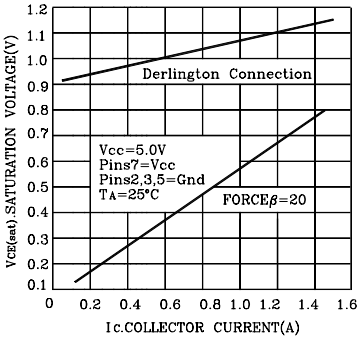


FIGURE 5.CURRENT LIMIT SENSE VOLTAGE versus TEMPERATURE

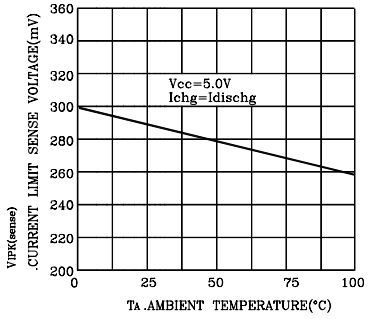


FIGURE 6.STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

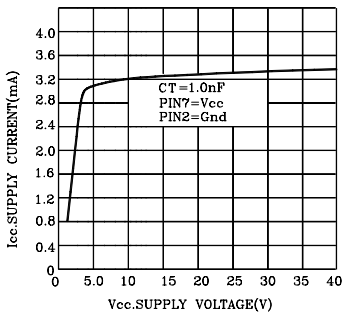


FIGURE 1.STEP-UP CONVERTER

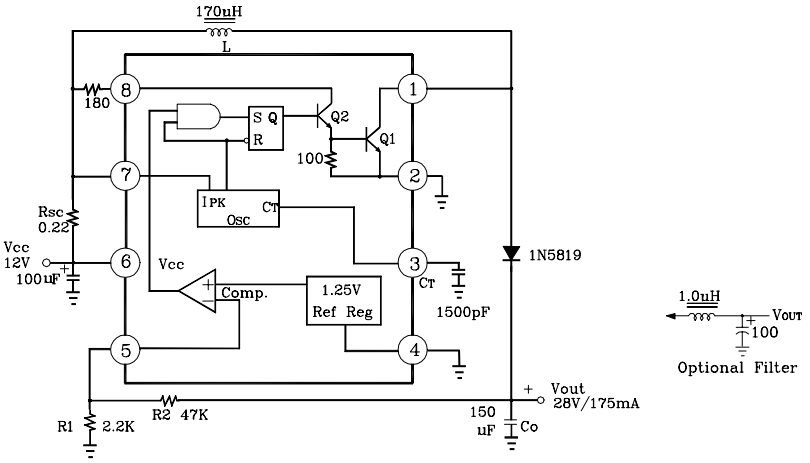
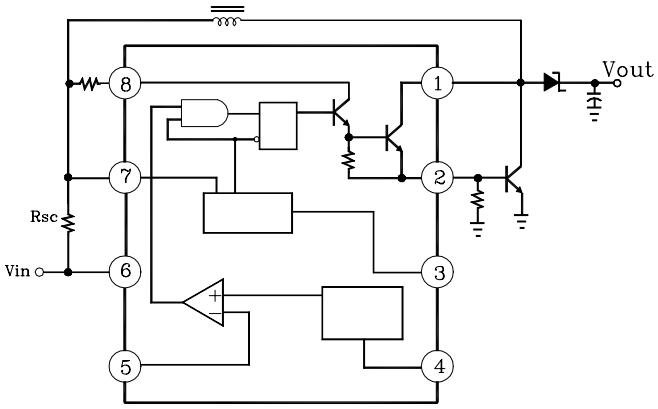
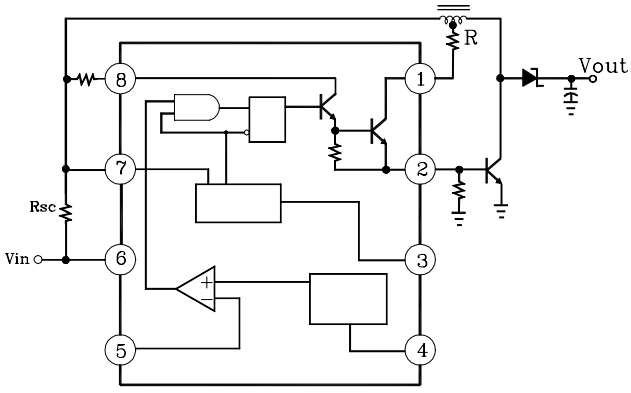


FIGURE 2.EXTERNAL CURRENT BOOST CONNECTIONS FOR Ic PEAK GREATER THAN 1.5A
2a.EXTERNAL NPN SWITCH **2b.EXTERNAL NPN SATURATED SWITCH**





Note:R→0 for constant Vin

FIGURE 3.STEP-DOWN CONVERTER

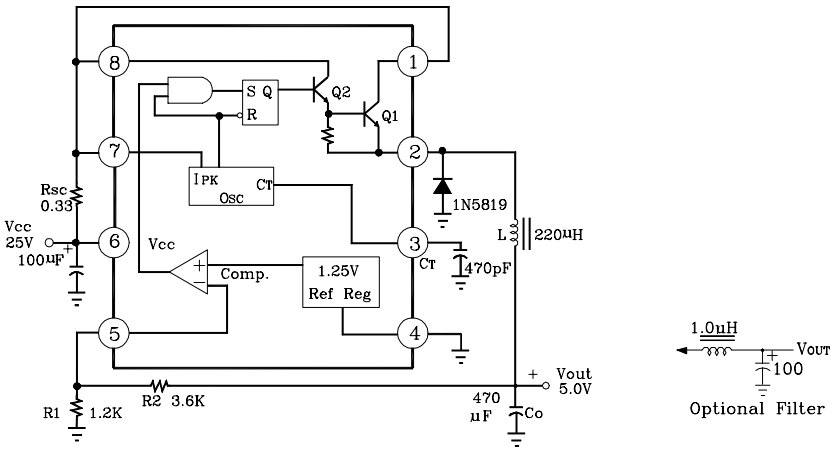
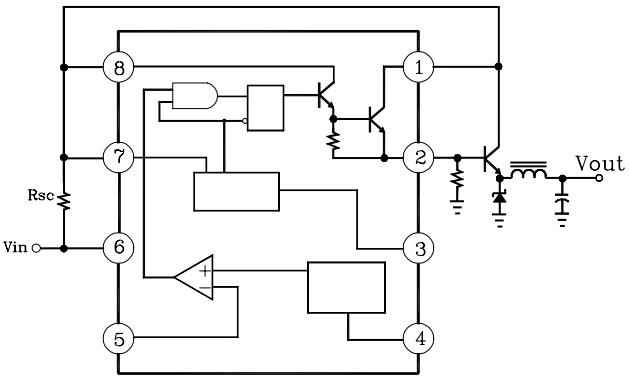


FIGURE 4.EXTERNAL CURRENT BOOST CONNECTIONS FOR Ic PEAK GREATER THAN 1.5A

4a.EXTERNAL NPN SWITCH



4b.EXTERNAL NPN SWITCH

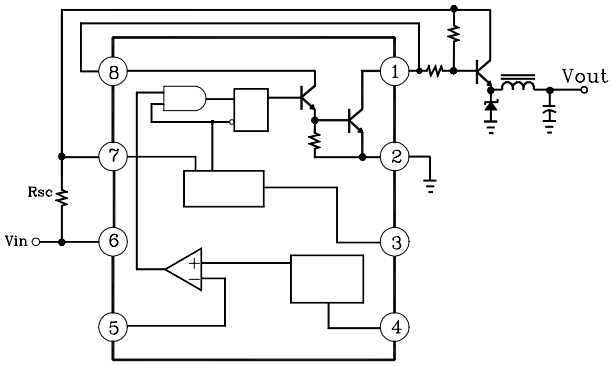


FIGURE 5.VOLTAGE INVERTING CONVERTER

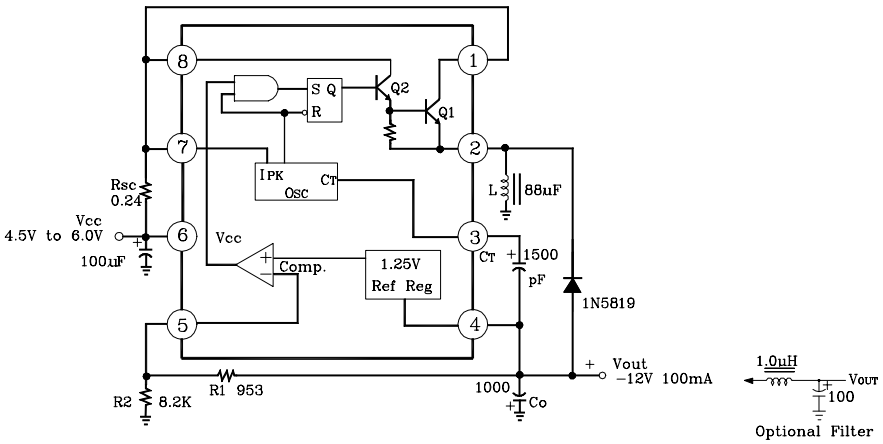
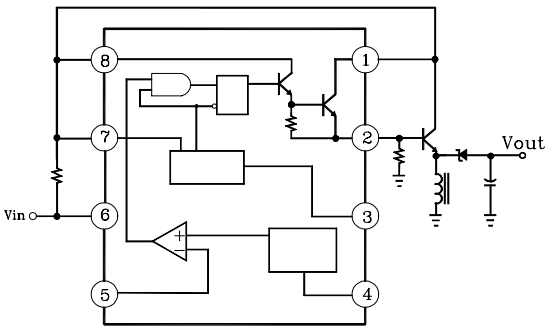
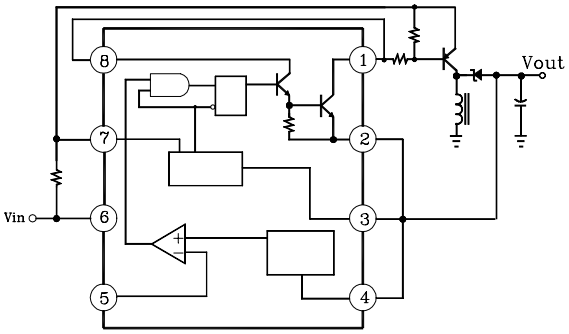


FIGURE 6.EXTERNAL CURRENT BOOST CONNECTIONS FOR Ic PEAK GREATER THAN 1.5A

6a.EXTERNAL NPN SWITCH



6b.EXTERNAL NPN SATURATED SWITCH



Calculation	Step-Up	Step-Down	Voltage-Inverting
ton toff	$\frac{Vout+V_F-Vin(min)}{V_{CC}(min)-Vsat-Vout}$	$\frac{V_{OUT}+V_F}{V_{CC}(min)-Vsat-Vout}$	$\frac{\lvert Vout \rvert +V_F}{V_{CC}+Vsat}$
(ton+toff) max	$\frac{1}{f\ min}$	$\frac{1}{f\ min}$	$\frac{1}{f\ min}$
C_T	4.0×10^{-5} ton	4.0×10^{-5} ton	4.0×10^{-5} ton
I_{pk}(switch)	$2Iout(max)\left(\frac{ton}{toff}+1\right)$	2Iout(max)	$2Iout(max)\left(\frac{ton}{toff}+1\right)$
Rsc	$0.3/I_{PK}$(switch)	$0.3/I_{PK}$(switch)	$0.3/I_{PK}$(switch)
L (min)	$\left(\frac{Vin(\min)-Vsat}{Ipk(switch)}\right)\cdot ton(\max)$	$\left(\frac{Vin(\min)-Vsat-Vout}{Ipk(switch)}\right)\ ton(\max)$	$\left(\frac{Vin(\min)-Vsat}{Ipk(switch)}\right)\ ton(\max)$
Co	$\left(\frac{Ioutton}{Vripple(pp)}\right)$	$\left(\frac{Ipk(switch)(ton+toff)}{8Vripple(pp)}\right)$	$\left(\frac{Ioutton}{Vripple(pp)}\right)$

TERMS AND DEFINITIONS

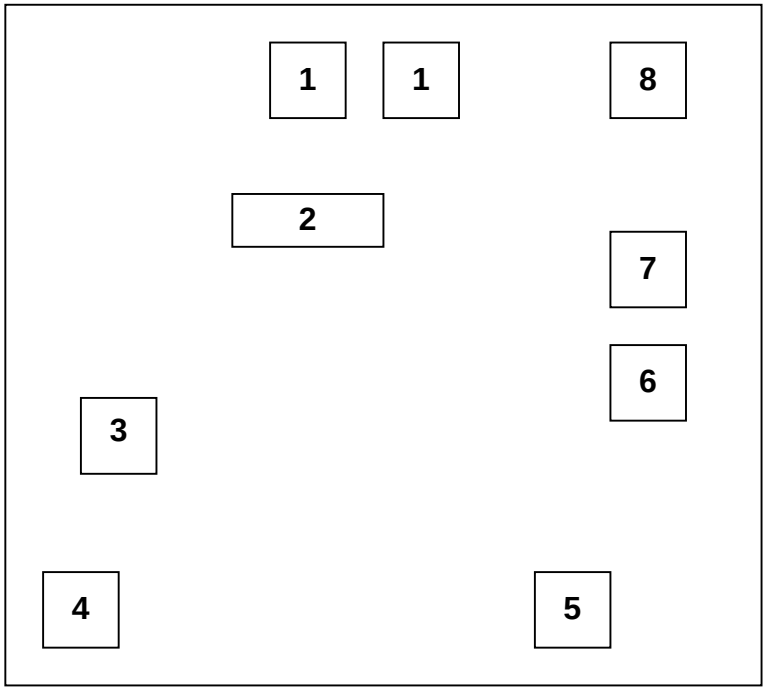
- Vsat = Saturation Voltage of the output switch.
- V_F = Forward Voltage drop of the rectifier.

The following power supply characteristics must be chosen:

- V_{in}= Normal input voltage
- Vout: Desied Output voltage, $\lvert Vout \rvert = 1.25\ (1+\frac{R2}{R1})$
- Iout : Desired output current.
- fmin : Minimum desired output switching frequency at the selected values for V_{in} and.Io.
- Vripple(p-p): Desired peak-to-peak output ripple voltage. in practice, the calculated capaitor value will need to be increased due to its equivalent series resistance and board layout.

  The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

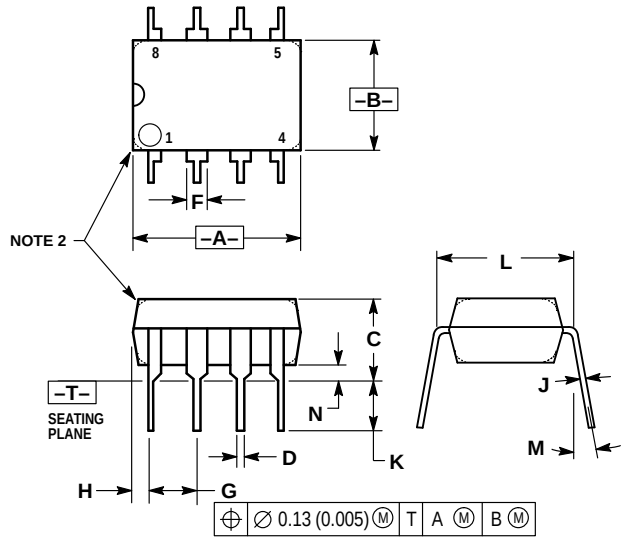
PAD LOCATION WS34063A (NEW DESIGN)



Chip Size: 1.72X1.82 mm

PAD No.	PAD NAME
1	Switch Collector *1
2	Switch Emitter *1
3	Timing Capacitor
4	GND
5	Comparator Inverting Input
6	V_{CC}
7	I_{PK} Sense
8	Driver Collector

***1: Two wires must be connected to 1 and 2 pin**



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040