FP1189

½ Watt HFET

The Communications Edge ™

Preliminary Product Information

Product Features

- DC – 4000 MHz
- +28 dBm P1dB
- +40 dBm Output IP3
- High Drain Efficiency
- 17 dB Gain @ 1900 MHz
- MTBF >100 Years
- SOT-89 SMT Package

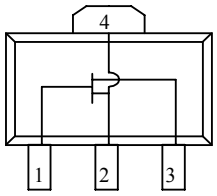
Product Description

The FP1189 is a high performance ½-Watt HFET (Heterostructure FET) in a low-cost SOT-89 surface-mount package. This device works optimally at a drain bias of +8 V and 100 mA to achieve +40 dBm output IP3 performance and an output power of +28 dBm at 1-dB compression.

The device conforms to WJ Communications' long history of producing high reliability and quality components. The FP1189 has an associated MTBF of over 100 years at a mounting temperature of 85° C. All devices are 100% RF & DC tested.

The product is targeted for use as driver amplifiers for wireless infrastructure where high performance and high efficiency is required.

Functional Diagram



Function	Pin No.
Input	1
Ground	2
Output/Bias	3
Ground	4

Specifications

DC Electrical Parameter	Units	Min	Typ	Max
Saturated Drain Current[1], I_{dss}	mA		300	
Transconductance, G_m	mS		175	
Pinch Off Voltage[2], V_p	V		-2.0	

Parameters[3]	Units	Min	Typ	Max
Frequency Range	MHz	DC		4000
Small Signal Gain, Gss	dB		17	
Output P1dB	dBm		+28	
Output IP3[4]	dBm		+40	
Thermal Resistance	°C/W			70

1. I_{dss} is measured with V_{gs} = 0 V, V_{ds} = 3 V.
2. Pinch-off voltage is measured when I_{ds} = 0.8 mA.
3. Test conditions unless otherwise noted: T = 25ºC, V_{DS} = 8 V, I_{DQ} = 100 mA, frequency = 1960 MHz in an application circuit with $Z_L = Z_{LOPT}$, $Z_S = Z_{SOPT}$.
4. 3OIP measured with two tones at an output power of +15 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Typical Parameters

Parameter	Units	Typical		
Frequency	MHz	900	1960	2140
S21	dB	TBD	16.5	17
S11	dB	TBD	-23	-30
S22	dB	TBD	-6	-7
Output P1dB	dBm	TBD	+28	+28
Output IP3	dBm	TBD	+40	+40
Noise Figure	dB	TBD	3.8	3.9
Drain Voltage	V	TBD	+8.0	+8.0
Drain Current	mA	TBD	100	100

1. The drain current is the quiescent current at small signal output levels. The current may increase as the output power is increased near its compression point.

Absolute Maximum Ratings

Parameters	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-40 to +125 °C
Maximum DC Power	2 W
RF Input Power (continuous)	+20 dBm

Operation of this device above any of there parameters may cause permanent damage

Ordering Information

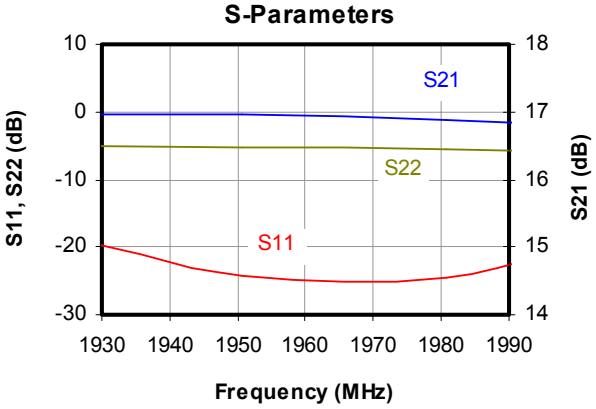
Part No.	Description
FP1189	½-Watt HFET (Available in Tape & Reel)
FP1189-PCB-900	900 MHz Application Circuit
FP1189-PCB-1900	1900 MHz Application Circuit

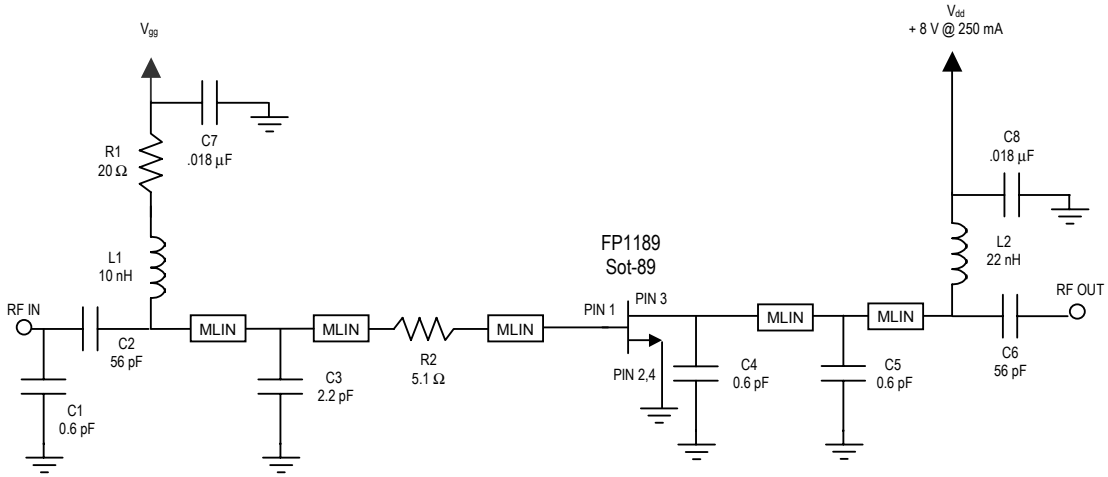
Application Circuit: 1960 MHz

Typical Specifications

Frequency	1960
S21 - Gain	16.5 dB
S11 - Input R.L.	-23 dB
S22 - Output R.L.	-6 dB
Output P1dB	+28 dBm
Output IP3	+40 dBm
Noise Figure	3.8 dB
V_{dd}	+8.0 V
I_{dd} [1]	100 mA

1 I_{dd} is the quiescent current at small signal output levels. The current may increase as the output power is increased near its compression point.

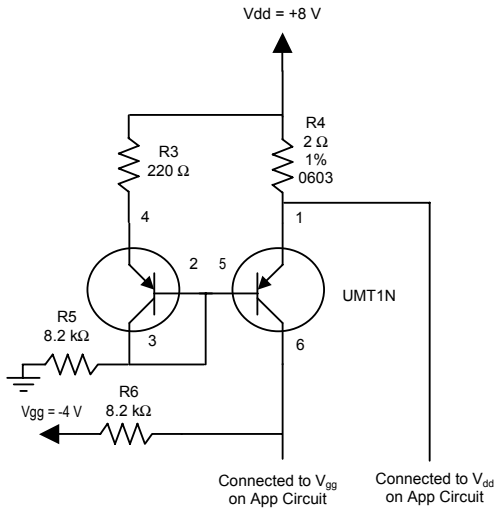




Application Note

Special attention should be taken to properly bias up the HFETs. Power supply sequencing is required to prevent the device from operating at 100% I_{dss} for a prolonged period of time and possibly causing damage to the device. It is recommended that for the safest operation, the negative supply be "first on and last off." With a negative gate voltage present, the drain voltage can then be applied to the device. The gate voltage can then be adjusted to have the device be used at the proper quiescent bias condition.

An optional temperature-compensation active-bias circuit is recommended for use with the application circuit, which requires two standard voltage supplies +8V and -4V, and is set for an optimal drain bias of +8V @ 100 mA. The circuit schematic, shown on the right, uses dual PNP transistors to provide a constant drain current into the FET and also eliminating the effects of pinchoff variation. Temperature compensation is achieved by tracking the voltage variation with the temperature of the emitter-to-base junction of the PNP transistors. Thus the transistor emitter voltage adjusts the voltage incident at the gate of the FET so that the device draws a constant current, regardless of the temperature. Two fixed voltage supplies are needed for operation. A Rohm dual transistor, UMT1N, and a dual-chip resistor (8.2 kΩ) are recommended to minimize board space and help decrease the current variability through R4 with the components being matched to one another. The active-bias circuit can directly be attached to the voltage supply ports in the circuit diagram as shown above (V_{dd} and V_{gg}).



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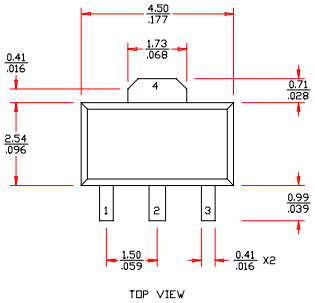
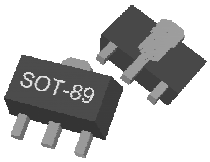
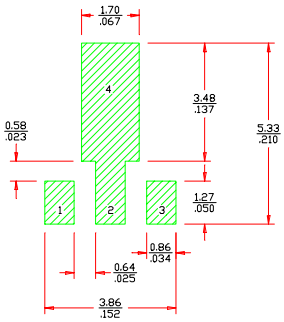
OUTLINE DRAWING





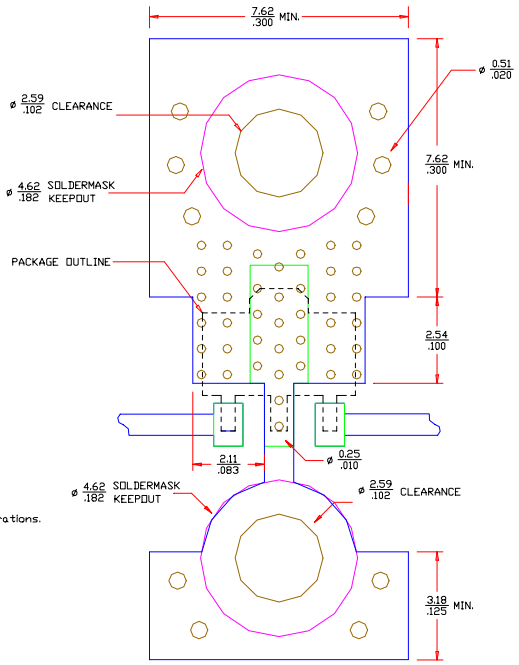
mm
inch

LAND PATTERN



FUNCTION	PIN NO.
INPUT	1
GROUND	2
OUTPUT (BIAS)	3
GROUND	4

MOUNTING CONFIGURATION



Notes: 1. Ground vias are critical for thermal and RF grounding considerations.
2. Trace width depends on PC board.
3. A minimum of 1 oz. / 1 oz. copper should be used.