## FEATURES

- **Dual 8-bit voltage output DAC**
- **Single supply from 2.7V to 5.5V**
- **Low supply current**
  - **0.8mA typical in slow mode**
  - **1.8mA typical in fast mode**
- **DNL ±0.2 LSB, INL ±0.5 LSB (max)**
- **Monotonic over temperature**
- **DSP compatible serial interface**
- **Programmable settling time of 1µs or 3µs typical**
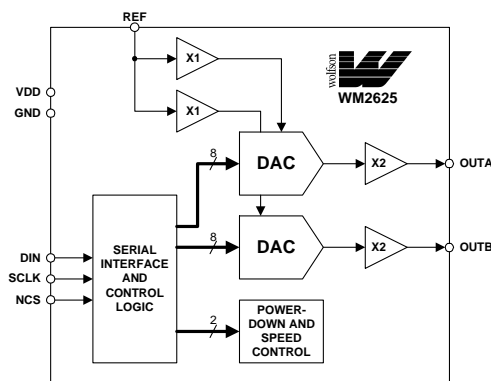- **High impedance reference input buffer**

## APPLICATIONS

- **Digital servo control loops**
- **Industrial process control**
- **Battery powered instruments and controls**
- **Machine and motion control devices**
- **Digital offset and gain adjustment**

## ORDERING INFORMATION

| DEVICE | TEMP. RANGE | PACKAGE |
|---|---|---|
| WM2625CD | 0° to 70°C | 8-pin SOIC |
| WM2625ID | -40° to 85°C | 8-pin SOIC |

## BLOCK DIAGRAM



## DESCRIPTION

The WM2625 is a dual 8-bit voltage output, resistor string digital-to-analogue converter. It can operate with supply voltages between 2.7V and 5.5V and can be powered down under software control. Power down reduces current consumption to 1µA.
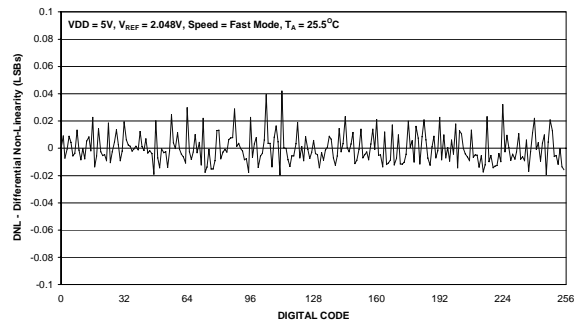
The device has been designed for glueless interface to industry standard microprocessors and DSPs. The WM2625 is programmed with a 16-bit serial word including 4 control bits and 8 data bits.

Excellent performance is delivered with a typical DNL of 0.2LSBs. Monotonicity is guaranteed over the operating temperature range. The settling time of the DAC is programmable to allow for optimisation of speed versus power dissipation. The analogue output is buffered by a rail-to-rail amplifier with a gain of two and a Class AB output stage.
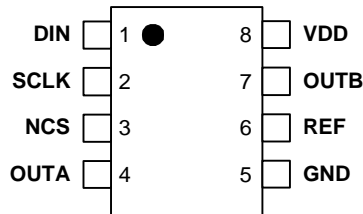
The reference voltage input features a high impedance buffer which eliminates the need to keep the reference source impedance low.

The WM2625 is available in an 8-pin SOIC package. Commercial (0° to 70°C) and Industrial (-40° to 85°C) temperature range variants are available.

## TYPICAL PERFORMANCE

## PIN CONFIGURATION

```
DIN   [  1 ●      8  ]  VDD
SCLK  [  2         7  ]  OUTB
NCS   [  3         6  ]  REF
OUTA  [  4         5  ]  GND
```

## PIN DESCRIPTION

| PIN NO | NAME | TYPE | DESCRIPTION |
|--------|------|------|-------------|
| 1 | DIN | Digital input | Serial data input |
| 2 | SCLK | Digital input | Serial clock input |
| 3 | NCS | Digital input | Chip select. This pin is active low. |
| 4 | OUTA | Digital input | DAC A analogue voltage output |
| 5 | GND | Supply | Ground |
| 6 | REF | Analogue input | Voltage reference input |
| 7 | OUT | Analogue output | DAC B analogue voltage output |
| 8 | VDD | Supply | Positive power supply |

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

| CONDITION | | MIN | MAX |
|-----------|--|-----|-----|
| Supply voltage, VDD to GND | | | 7V |
| Digital input voltage | | -0.3V | VDD + 0.3V |
| Reference input voltage | | -0.3V | VDD + 0.3V |
| Operating temperature range, $T_A$ | WM2625CD | 0°C | 70°C |
|  | WM2625ID | -40°C | 85°C |
| Storage temperature | | -65°C | 150°C |
| Soldering lead temperature, 1.6mm (1/16 inch) from package body for 10 seconds | | | 260°C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------|-----------------|-----|-----|-----|------|
| Supply voltage | VDD | | 2.7 | | 5.5 | V |
| High-level digital input voltage | $V_{IH}$ | VDD = 2.7V to 5.5V | 2 | | | V |
| Low-level digital input voltage | $V_{IL}$ | VDD = 2.7V to 5.5V | | | 0.8 | V |
| Reference voltage to REF pin | $V_{REF}$ | See Note | GND | | VDD - 1.5 | V |
| Load resistance | $R_L$ | | 2 | | | kΩ |
| Load capacitance | $C_L$ | | | | 100 | pF |
| Serial clock frequency | $f_{SCLK}$ | | | | 20 | MHz |
| Operating free-air temperature | $T_A$ | WM2625CD | 0 | | 70 | °C |
|  | | WM2625ID | -40 | | 85 | °C |

**Note:** Reference input voltages greater than VDD/2 will cause clipping for large DAC codes.

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# ELECTRICAL CHARACTERISTICS

**Test Conditions:**

$R_L$ = 10kΩ, $C_L$ = 100pF. VDD = 5V ±10%, $V_{REF}$ = 2.048V and VDD = 3V ±10%, $V_{REF}$ = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Static DAC Specifications** | | | | | | |
| Resolution | | | 8 | | | bits |
| Integral non-linearity | INL | See Note 1 | | ±0.3 | ±0.5 | LSB |
| Differential non-linearity | DNL | See Note 2 | | ±0.07 | ±0.2 | LSB |
| Zero code error | ZCE | See Note 3 | | | ±12 | mV |
| Gain error | GE | See Note 4 | | | ±0.5 | % FSR |
| D.C. power supply rejection ratio | D.C. PSRR | See Note 5 | | -65 | | mV/V |
| Zero code error temperature coefficient | | See Note 6 | | 10 | | ppm/°C |
| Gain error temperature coefficient | | See Note 6 | | 10 | | ppm/°C |
| **DAC Output Specifications** | | | | | | |
| Output voltage range | | | 0 | | VDD - 0.4 | V |
| Output load regulation | | 2kΩ to 10kΩ load See Note 7 | | | 0.29 | % FS |
| **Power Supplies** | | No load, DAC value = 128, all digital inputs 0V or VDD | | | | |
| Active supply current | $I_{DD}$ | Slow Mode | | 0.8 | 1 | mA |
| | | Fast Mode | | 1.8 | 2.3 | mA |
| Power down supply current | | See Note 8 | | 1 | 3 | µA |
| **Dynamic DAC Specifications** | | | | | | |
| Slew rate | SR | DAC output 10%-90% Slow Fast See Note 9 | | 0.5 3 | | V/µs V/µs |
| Full-scale settling time | $t_s$ | DAC output 10%-90% Slow Fast See Note 10 | | 3 1 | 10 3 | µs µs |
| Glitch energy | | DIN = 0 to 1, $f_{CLK}$ = 100kHz, NCS = VDD | | 5 | | nV-s |
| Signal to noise ratio | SNR | $f_s$ = 102kSPS, $f_{OUT}$ = 1kHz, See Note 11 | 52 | 54 | | dB |
| Signal to noise and distortion ratio | SINAD | | 48 | 49 | | dB |
| Total harmonic distortion | THD | | | -50 | -48 | dB |
| Spurious free dynamic range | SFDR | | 48 | 50 | | dB |
| **Reference** | | | | | | |
| Reference input resistance | $R_{REFIN}$ | | | 10 | | MΩ |
| Reference input capacitance | $C_{REFIN}$ | | | 5 | | pF |
| Reference feedthrough | | $V_{REF}$ = 1$V_{PP}$ at 1kHz + 1.024V dc, DAC code 0 | | -80 | | dB |
| Reference input bandwidth | | $V_{REF}$ = 0.2$V_{PP}$ + 1.024V dc Slow Fast | | 0.525 1.3 | | MHz MHz |
| **Digital Inputs** | | | | | | |
| High level input current | $I_{IH}$ | Input voltage = VDD | -1 | | 1 | µA |
| Low level input current | $I_{IL}$ | Input voltage = 0V | -1 | | 1 | µA |
| Input capacitance | $C_I$ | | | 8 | | pF |

**Notes:**

1. **Integral non-linearity** (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full scale errors).

2. **Differential non-linearity** (DNL) is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage always changes in the same direction (or remains constant) as the digital input code.

3. **Zero code error** is the voltage output when the DAC input code is zero.

4. **Gain error** is the deviation from the ideal full-scale output excluding the effects of zero code error.

5. **Power supply rejection ratio** is measured by varying VDD from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.

6. **Zero code error** and **Gain error** temperature coefficients are normalised to full-scale voltage.

7. **Output load regulation** is the difference between the output voltage at full scale with a 10kΩ load and 2kΩ load. It is expressed as a percentage of the full scale output voltage with a 10kΩ load.

8. **$I_{DD}$** is measured while continuously writing code 128 to the DAC. For $V_{IH} < $ VDD - 0.7V and $V_{IL} > 0.7$V supply current will increase.

9. **Slew rate** results are for the lower value of the rising and falling edge slew rates

10. **Settling time** is the time taken for the signal to settle to within 0.5LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.

11. **SNR, SNRD, THD** and **SPFDR** are measured on a synthesised sine wave at frequency $f_{OUT}$ generated with a sampling frequency $f_s$.
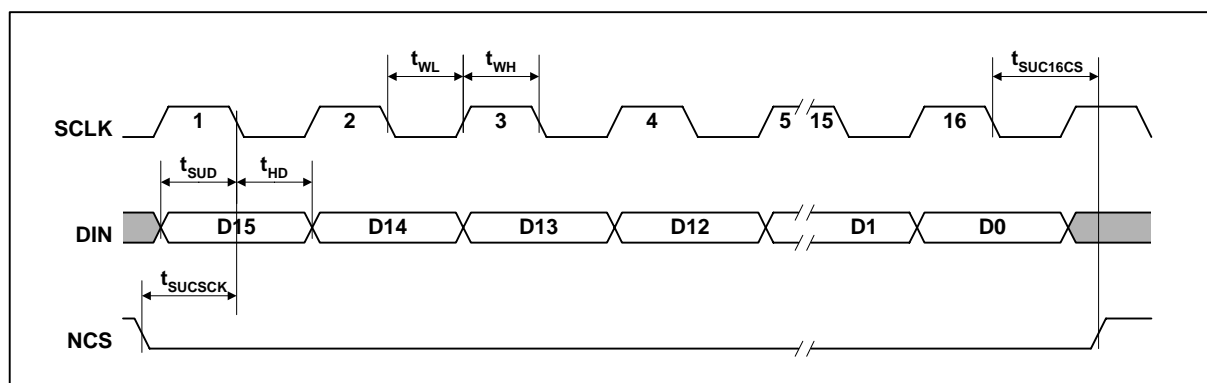
## SERIAL INTERFACE



**Figure 1  Timing Diagram**

**Test Conditions:**
$R_L$ = 10kΩ, $C_L$ = 100pF. VDD = 5V ± 10%, $V_{REF}$ = 2.048V and VDD = 3V ± 10%, $V_{REF}$ = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

| SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------|-----------------|-----|-----|-----|------|
| $t_{SUCSCK}$ | Setup time, NCS low before first falling SCLK edge | 10 | | | ns |
| $t_{SUC16CS}$ | Setup time, 16th falling SCLK edge (when data bit D0 is sampled) before NCS rising edge. | 10 | | | ns |
| $t_{WH}$ | Pulse duration, SCLK high. | 25 | | | ns |
| $t_{WL}$ | Pulse duration, SCLK low. | 25 | | | ns |
| $t_{SUD}$ | Setup time, data ready before SCLK falling edge. | 10 | | | ns |
| $t_{HD}$ | Hold time, data held valid after SCLK falling edge. | 10 | | | ns |

## TYPICAL PERFORMANCE GRAPHS
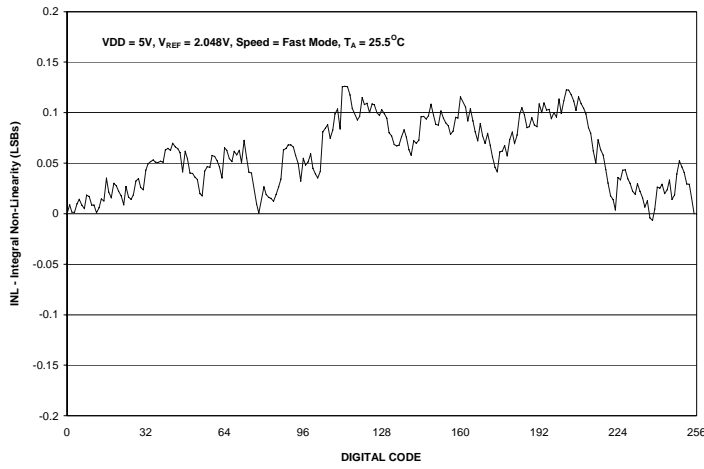


**Figure 2  Integral Non-Linearity**
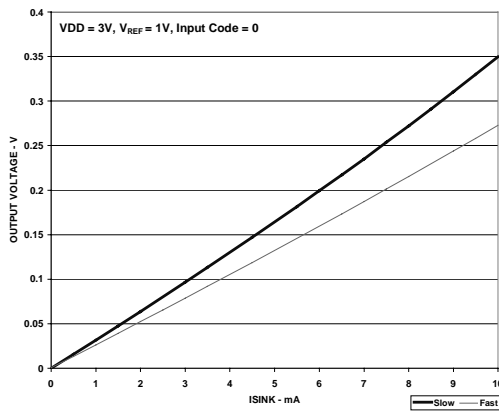


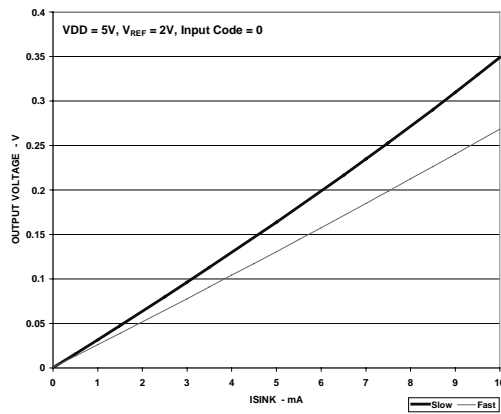**Figure 3  Sink Current VDD = 3V**
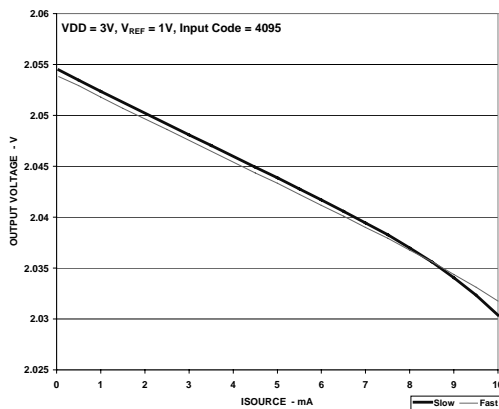


**Figure 4  Sink Current VDD = 5V**



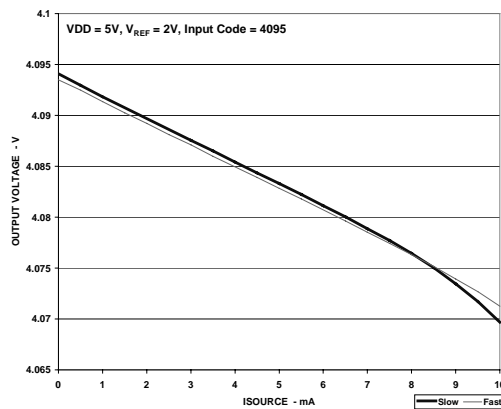**Figure 5  Source Current VDD = 3V**



**Figure 6  Source Current VDD = 5V**

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# DEVICE DESCRIPTION

## GENERAL FUNCTION

The WM2625 is a dual 8-bit, voltage output DAC operating from a single supply. It uses a resistor string network buffered with an op amp to convert 8-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference input voltage and the input code according to the following relationship:

$$V_{out} = 2(V_{REFIN})\frac{CODE}{256}$$

| INPUT | | OUTPUT |
|---|---|---|
| 1111 | 1111 | $2(V_{REF})\dfrac{255}{256}$ |
| : | | : |
| 1000 | 0001 | $2(V_{REF})\dfrac{129}{256}$ |
| 1000 | 0000 | $2(V_{REF})\dfrac{128}{256} = V_{REF}$ |
| 0111 | 1111 | $2(V_{REF})\dfrac{127}{256}$ |
| : | | : |
| 0000 | 0001 | $2(V_{REF})\dfrac{1}{256}$ |
| 0000 | 0000 | 0V |

**Table 1  Binary Code Table (0V to 2V$_{REF}$ Output), Gain = 2**

### POWER ON RESET

An internal power-on-reset circuit resets the DAC register to all 0s on power-up.

### BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

### EXTERNAL REFERENCE

The reference voltage input is buffered which makes the DAC input resistance independent of code. The REF pin has an input resistance of 10MΩ and an input capacitance of typically 5pF. The reference voltage determines the DAC full-scale output.

## SERIAL INTERFACE

Before writing any data to the WM2625, the interface must be enabled by setting NCS to low. Incoming data on DIN (starting with the MSB) is then shifted bit-per-bit into the internal register on the falling edges of SCLK. From there data is loaded into the target latch after 16 bits have been transferred, or when NCS rises. Three internal latches can be addressed: DAC A, DAC B, or the buffer latch. This makes it possible to update both DACs simultaneously or to update one independently of the other (see 'Addressing the Buffer and DAC Latches', below).

### SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the device timing. The maximum serial rate is:

$$f_{SCLK\,max} = \frac{1}{t_{WH\,min} + t_{WL\,min}} = 20MHz$$

Since a data word contains 16 bits, the sample rate for one channel is limited to

$$f_{s\max} = \frac{1}{16 \times (t_{WH\min} + t_{WL\min})} = 1.25 MHz$$

For full two-channel operation, where two data words need to be transmitted per sample, this figure is halved to 625kHz. However, the DAC settling time to 8-bit accuracy limits the response time of the analogue output for large input step transitions.

## SOFTWARE CONFIGURATION OPTIONS

Table 2 shows the composition of a 16-bit data word. D11-D4 contains the 8-bit data word, and D14-D13 hold the programmable options. Bits D15 and D12 are used for addressing the different latches. D3 to D0 are unused and should be set to ZERO.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| R1 | SPD | PWR | R0 | New DAC value (8 bits) | | | | | | | | 0 | 0 | 0 | 0 |

**Table 2  Register Map**

### PROGRAMMABLE CONVERTER SPEED

SPD (Bit 14) allows for software control of the converter speed. A ONE selects the fast mode, where typical settling time to within ±0.5LSB of the final value is 1μs. a ZERO puts the device into the slow mode, where typical settling time is 3μs.

### PROGRAMMABLE POWER DOWN

The power down function is controlled by PWR (Bit 13). A ZERO configures the device as active, or fully powered up, a ONE sets the device into power down mode. When the power down function is released the device reverts to the DAC code set prior to power down.

### ADDRESSING THE BUFFER AND DAC LATCHES

Data received on the serial interface is routed according to the values of bits R1 and R0, as shown in Table 3

| R1 (BIT D15) | R0 (BIT D12) | REGISTER |
|:---:|:---:|:---|
| 0 | 0 | Write data to DAC B and buffer |
| 0 | 1 | Write data to buffer |
| 1 | 0 | Write data to DAC A and update DAC B with buffer content |
| 1 | 1 | Reserved |

**Table 3  Latch Addressing**

To update both DACs simultaneously, the data intended for DAC B should first be stored in the buffer. Subsequently, writing data to DAC A will automatically update the DAC B latch from the buffer, so that the analogue output of both DACs will change at the same time.

When updating the two channels independently, all data written to the DAC B latch (R1 and R0 set to ZERO) is also copied to the buffer. Thus the automatic update of DAC B when writing to DAC A latch (R1=1, R0=0) does not change the DAC B data. Data should not be written only to the buffer when operating in this mode.

### EXAMPLES OF OPERATION

*Simultaneous operation, slow mode:*

1. Write data for DAC B to buffer

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 1 | New DAC B value | | | | | | | | 0 | 0 | 0 | 0 |

2. Write new DAC A value and update DAC B from buffer simultaneously

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 0 | 0 | 0 | New DAC A value | | | | | | | | 0 | 0 | 0 | 0 |

*Independent operation, fast mode:*

Set DAC B output (fast mode):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | | | | New DAC B value | | | | | 0 | 0 | 0 | 0 |

Set DAC A output (fast mode):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 0 | | | | New DAC A value | | | | | 0 | 0 | 0 | 0 |

# APPLICATIONS INFORMATION

## LINEARITY, OFFSET, AND GAIN ERROR

Amplifiers operating from a single supply can have positive or negative voltage offsets. With a positive offset, the output voltage changes on the first code transition. However, if the offset is negative, the output voltage may not change with the first code, depending on the magnitude of the offset voltage. This is because with the most negative supply rail being ground, any attempt to drive the output amplifier below ground will clamp the output at 0 V. The output voltage then remains at zero until the input code is sufficiently high to overcome the negative offset voltage, resulting in the transfer function shown in Figure 7.
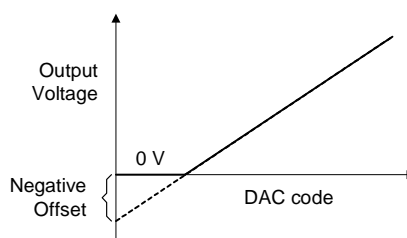


**Figure 7  Effect of Negative Offset**

This offset error, not the linearity error, produces the breakpoint. The transfer function would follow the dotted line if the output buffer could drive below the ground rail.

DAC linearity is measured between zero-input code (all input bits at 0) and full-scale code (all inputs at 1), disregarding offset and full-scale errors. However, due to the breakpoint in the transfer function, single supply operation does not allow for adjustment when the offset is negative. In such cases, the linearity is therefore measured between full-scale and the lowest code that produces a positive (non-zero) output voltage.

## POWER SUPPLY DECOUPLING AND GROUNDING

Printed circuit boards with separate analogue and digital ground planes deliver the best system performance. The two ground planes should be connected together at the low impedance power supply source. Ground currents should be managed so as to minimise voltage drops across the ground planes.

A 0.1µF decoupling capacitor should be connected between the positive supply and ground pins of the DAC, with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analogue supply from the digital supply.

## PACKAGE DIMENSIONS

**D: 8 PIN SOIC  3.9mm  Wide Body**

**DM009.B**
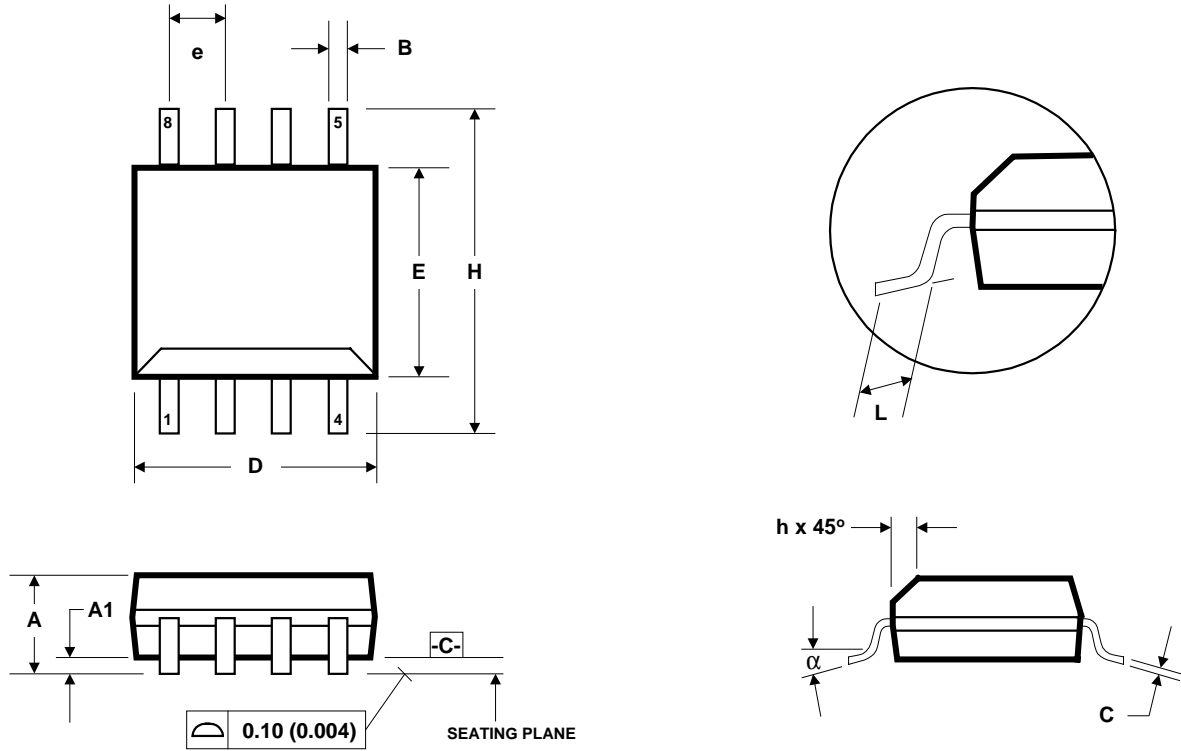


| Symbols | Dimensions (mm) | | Dimensions (Inches) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.0532 | 0.0688 |
| A$_1$ | 0.10 | 0.25 | 0.0040 | 0.0098 |
| B | 0.33 | 0.51 | 0.0130 | 0.0200 |
| C | 0.19 | 0.25 | 0.0075 | 0.0098 |
| D | 4.80 | 5.00 | 0.1890 | 0.1968 |
| e | 1.27 BSC | | 0.050 BSC | |
| E | 3.80 | 4.00 | 0.1497 | 0.1574 |
| h | 0.25 | 0.50 | 0.0099 | 0.0196 |
| H | 5.80 | 6.20 | 0.2284 | 0.2440 |
| L | 0.40 | 1.27 | 0.0160 | 0.0500 |
| α | 0° | 8° | 0° | 8° |
| | | | | |
| REF: | JEDEC.95, MS-012 | | | |

NOTES:
A.  ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B.  THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C.  BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D.  MEETS JEDEC.95 MS-012, VARIATION = AA.  REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.