WM2632
Octal 8-bit, Serial Input, Voltage Output DAC with Internal Reference

Production Data, April 2001, Rev 1.1

FEATURES

- **Eight 8-bit DACs in one package**
- **Dual supply 2.7V to 5.5V operation**
- **DNL ±0.1 LSBs, INL ±0.3 LSBs typical**
- **Programmable settling time / power (1.0μs typical in fast mode)**
- **Internal programmable voltage reference**
- **Microcontroller compatible serial interface**
- **Power down mode (< 0.1μA)**
- **Monotonic over temperature**
- **Data output for daisy chaining**

APPLICATIONS

- **Battery powered test instruments**
- **Digital offset and gain adjustment**
- **Battery operated / remote industrial controls**
- **Programmable loop controllers**
- **CNC machine tools**
- **Machine and motion control devices**
- **Wireless telephone and communication systems**
- **Robotics**

DESCRIPTION

The WM2632 is an octal, 8-bit, resistor string digital-to-analogue converter. The eight individual DACs contained in the IC can be switched in pairs between fast and slow (low power) operation modes, or powered down, under software control. Alternatively, the whole device can be powered down, reducing current consumption to less than 0.1μA.

The DAC outputs are buffered by a rail-to-rail amplifier with a gain of two, which is configurable as Class A (fast mode) or Class AB (for low-power mode).

The WM2632 has been designed to interface directly to industry standard microprocessors and DSPs, and can operate on two separate analogue and digital power supplies. It is programmed with a 16-bit serial word comprising 4 address bits and up to 12 DAC or control register data bits. All eight DACs can be simultaneously forced to a preset value using a preset input pin.

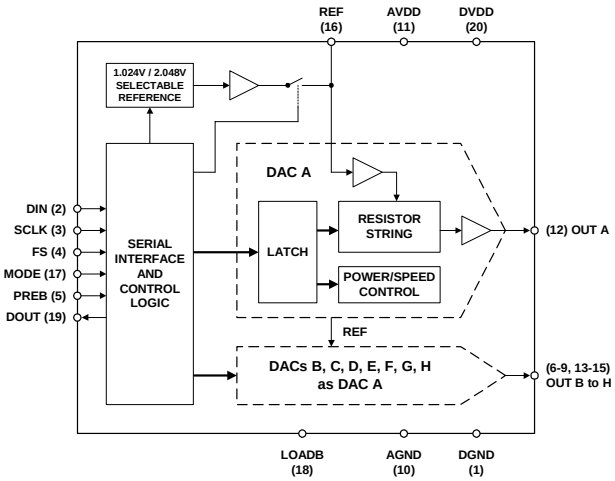
A daisy-chain data output makes it possible to control several of Wolfson's octal DACs from the same interface, without increasing the number of control lines.

The device is available in a 20-pin TSSOP package. Commercial temperature (0° to 70°C) and Industrial temperature (-40° to 85°C) variants are supported.

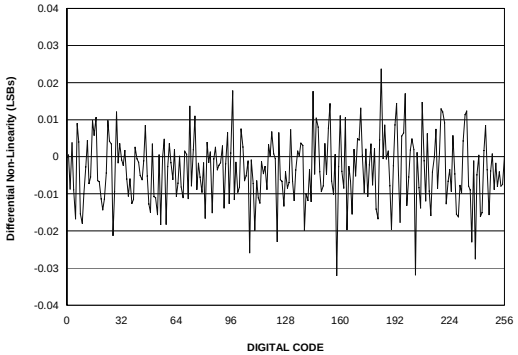
ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2632CDT	0° to 70°C	20-pin TSSOP
WM2632IDT	-40° to 85°C	20-pin TSSOP

BLOCK DIAGRAM

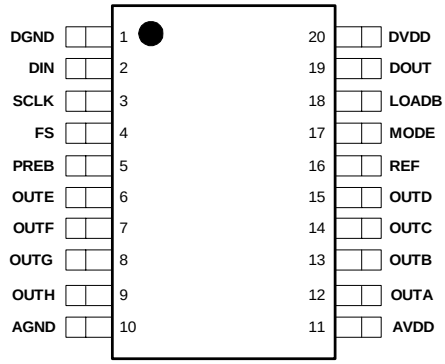


TYPICAL PERFORMANCE



WOLFSON MICROELECTRONICS LTD
Bernard Terrace, Edinburgh, EH8 9NX, UK
Tel: +44 (0) 131 667 9386
Fax: +44 (0) 131 667 5176
Email: sales@wolfson.co.uk
www.wolfsonmicro.com

PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	DGND	Supply	Digital Ground
2	DIN	Digital input	Digital serial data input
3	SCLK	Digital input	Serial clock input
4	FS	Digital input	Frame sync input
5	PREB	Digital input	Preset input
6	OUTE	Analogue output	DAC Output E
7	OUTF	Analogue output	DAC Output F
8	OUTG	Analogue output	DAC Output G
9	OUTH	Analogue output	DAC Output H
10	AGND	Supply	Analogue Ground
11	AVDD	Supply	Analogue positive power supply
12	OUTA	Analogue output	DAC Output A
13	OUTB	Analogue output	DAC Output B
14	OUTC	Analogue output	DAC Output C
15	OUTD	Analogue output	DAC Output D
16	REF	Analogue I/O	Voltage reference input / output
17	MODE	Digital input	Input mode
18	LOADB	Digital input	Load DAC
19	DOUT	Digital output	Serial data output
20	DVDD	Supply	Digital positive power supply

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION		MIN	MAX
Digital supply voltages, AVDD or DVDD to GND			7V
Reference input voltage		-0.3V	AVDD + 0.3V
Digital input voltage range to GND		-0.3V	DVDD + 0.3V
Operating temperature range, T_A	WM2632CDT WM2632IDT	0°C -40°C	70°C 85°C
Storage temperature		-65°C	150°C
Soldering lead temperature, 1.6mm (1/16 inch) from package body for 10 seconds			260°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	AVDD, DVDD		2.7		5.5	V
High-level digital input voltage	V_{IH}		2			V
Low-level digital input voltage	V_{IL}				0.8	V
Reference voltage to REF	V_{REF}	AVDD = 5V	GND	2.048	AVDD	
		AVDD = 3V	GND	1.024	AVDD	V
Output Load Resistance	R_L		2			kΩ
Load capacitance	C_L				100	pF
Operating free-air temperature	T_A	WM2632CDT	0		70	°C
		WM2632IDT	-40		85	°C

Note: Reference input voltages greater than AVDD/2 will cause saturation for large DAC codes.

ELECTRICAL CHARACTERISTICS

Test Characteristics:
R_L = 10kΩ, C_L = 100pF AVDD = DVDD = 5V ± 10%, V_{REF} = 2.048V and AVDD = DVDD = 3V ± 10%, V_{REF} = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static DAC Specifications						
Resolution				8		bits
Integral non-linearity	INL	Code 6 to 255 (see Note 1)		±0.3	±1	LSB
Differential non-linearity	DNL	Code 6 to 255 (see Note 2)		±0.1	±1	LSB
Zero code error	ZCE	See Note 3			±30	mV
Gain error	GE	See Note 4			±0.6	% FSR
DC power supply rejection ratio	PSRR	See Note 5		-50		dB
Zero code error temperature coefficient		See Note 6		30		µV/°C
Gain error temperature coefficient		See Note 6		10		ppm/°C
DAC Output Specifications						
Output voltage range		10kΩ Load	0		AVDD-0.4	V
Output load regulation		2kΩ to 10kΩ load See Note 7			±0.3	% Full Scale
Power Supplies						
Active supply current	IDD	No load, V_{IH}=DVDD, V_{IL}=0V AVDD = DVDD = 5V, V_{REF} = 2.048V Slow Fast See Note 8		 6 16	 8 21	 mA mA
Power down supply current		No load, all inputs 0V or DVDD		0.1		µA
Dynamic DAC Specifications						
Slew rate		DAC code 10%-90% Load = 10kΩ, 100pF Fast Slow See Note 9	 4 1	 10 3		 V/µs V/µs
Settling time		DAC code 10%-90% Load = 10kΩ, 100pF Fast Slow See Note 10		 1 3	 3 7	 µs µs
Glitch energy		DAC code 127 to 128		4		nV-s
Channel Crosstalk		10kHz sine wave, 4V pk-pk		-90		dB

Test Characteristics:
R_L = 10kΩ, C_L = 100pF AVDD = DVDD = 5V ± 10%, V_{REF} = 2.048V and AVDD = DVDD = 3V ± 10%, V_{REF} = 1.024V over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Configured as Input						
Reference input resistance	R_{REF}			50		kΩ
Reference input capacitance	C_{REF}			10		pF
Reference feedthrough		V_{REF}=2V_{PP} at 1kHz + 2.048V DC, DAC code 0		-84		dB
Reference input bandwidth		V_{REF}= 0.4V_{PP} + 2.048V DC, DAC code 128 Slow Fast		 1.9 2.2		 MHz MHz
Reference Configured as Output						
Low reference voltage	$V_{REFOUTL}$		1.010	1.024	1.040	V
High reference voltage	$V_{REFOUTH}$	VDD > 4.75V	2.020	2.048	2.096	V
Output source current	I_{REFSRC}				1	mA
Output sink current	I_{REFSNK}		-1			mA
Load Capacitance		in parallel with 100nF cap.	1	10		µF
PSRR				60		dB
Digital Inputs						
High level input current	I_{IH}	Input voltage = DVDD	-1		1	µA
Low level input current	I_{IL}	Input voltage = 0V	-1		1	µA
Input capacitance	C_I			8		pF

Notes:

1. **Integral non-linearity (INL)** is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full scale errors).
2. **Differential non-linearity (DNL)** is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in digital input code.
3. **Zero code error** is the voltage output when the DAC input code is zero.
4. **Gain error** is the deviation from the ideal full-scale output excluding the effects of zero code error.
5. **Power supply rejection ratio** is measured by varying AVDD from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.
6. **Zero code error** and **Gain error** temperature coefficients are normalised to full-scale voltage.
7. **Output load regulation** is the difference between the output voltage at full scale with a 10kΩ load and 2kΩ load. It is expressed as a percentage of the full scale output voltage with a 10kΩ load.
8. **I_{DD}** is measured while continuously writing a digital code of 128 to the DAC. For V_{IH} < DVDD - 0.7V and V_{IL} > 0.7V supply current will increase.
9. **Slew rate results** are for the lower value of the rising and falling edge slew rates.
10. **Settling time** is the time taken for the signal to settle to within 0.5LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.

SERIAL INTERFACE

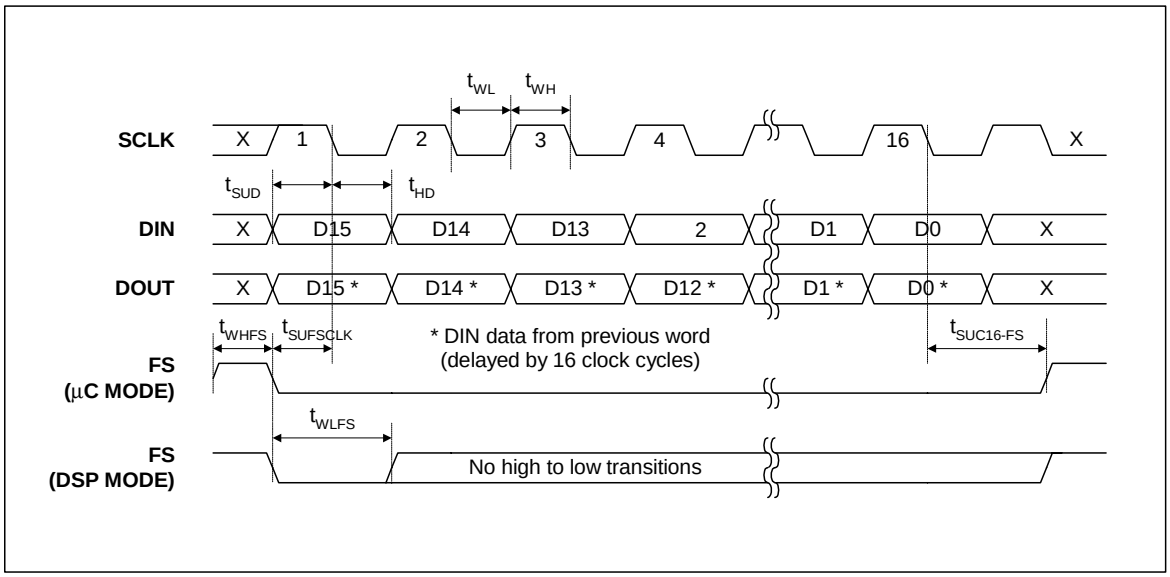


Figure 1 Timing Diagram

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SUFSCLK}$	Setup time, FS pin low before first falling edge of SCLK	8			ns
$t_{C16\text{-}FS}$	Setup time, 16th falling clock edge after FS low to rising edge of FS (only used in microcontroller mode)	10			ns
t_{WLOADB}	Pulse duration, LOADB low	10			ns
t_{WH}	Pulse duration, SCLK high	16			ns
t_{WL}	Pulse duration, SCLK low	16			ns
t_{SUD}	Setup time, data ready before SCLK falling edge	8			ns
t_{HD}	Hold time, data held valid after SCLK falling edge	5			ns
t_{WHFS}	Pulse duration, FS high	10			ns
t_{WLFS}	Pulse duration, FS low	10			ns
t_s	DAC Output settling time	see Dynamic DAC Specifications			

TYPICAL PERFORMANCE GRAPHS

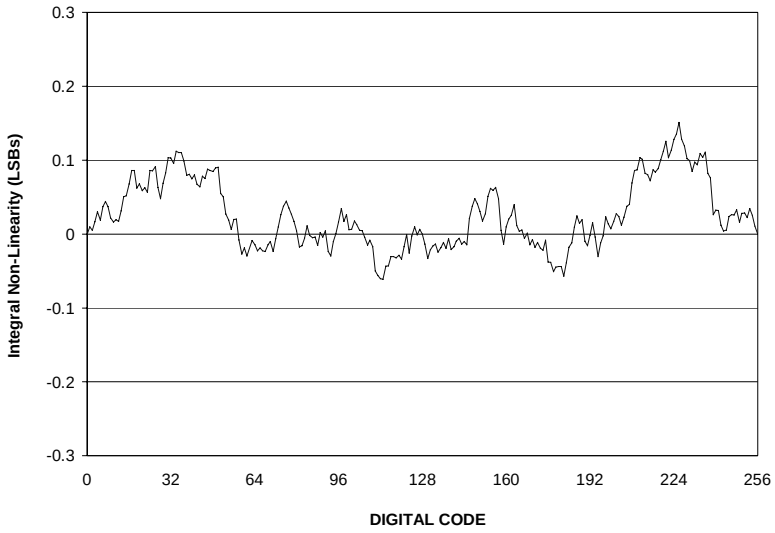


Figure 2 Integral Non-Linearity

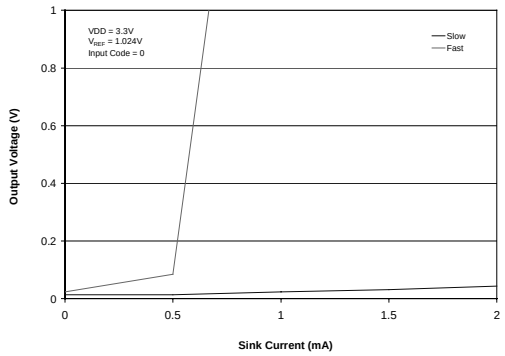


Figure 3 Output Load Regulation (Sink) AVDD = 3V

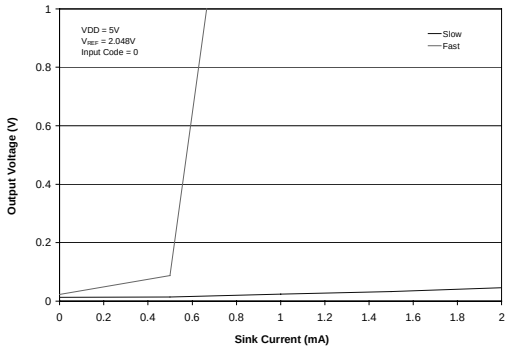


Figure 4 Output Load Regulation (Sink) AVDD = 5V

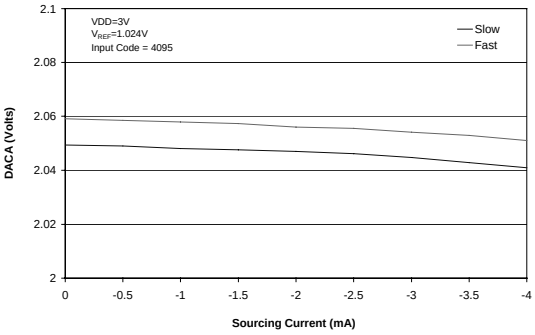


Figure 5 Output Load Regulation (Source) AVDD = 3V

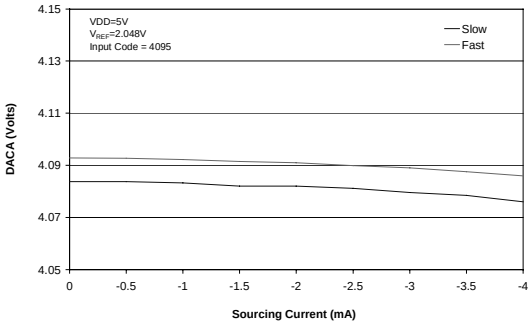


Figure 6 Output Load Regulation (Source) AVDD = 5V

DEVICE DESCRIPTION

GENERAL FUNCTION

The WM2632 is an octal 8-bit, voltage output DAC. It contains a serial interface, control logic for speed and power down, a programmable voltage reference, and eight digital to analogue converters. Each converter uses a resistor string network buffered with an op amp to convert 8-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference input voltage and the input code according to the following relationship:

$$\text{Output voltage} = 2\left(V_{REF}\right)\frac{CODE}{256}$$

INPUT	OUTPUT
1111 1111	$2\left(V_{REF}\right)\frac{255}{256}$
:	:
1000 0001	$2\left(V_{REF}\right)\frac{129}{256}$
1000 0000	$2\left(V_{REF}\right)\frac{128}{256} = V_{REF}$
0111 1111	$2\left(V_{REF}\right)\frac{127}{256}$
:	:
0000 0001	$2\left(V_{REF}\right)\frac{1}{256}$
0000 0000	0V

Table 1 Binary Code Table (0V to $2V_{REF}$ Output), Gain = 2

POWER ON RESET

An internal power-on-reset circuit resets the DAC register to all 0s on power-up.

BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

PROGRAMMABLE REFERENCE

The DAC reference can be sourced internally or externally under software control. If an external reference voltage is applied to the REF pin, the device must be configured to accept this. If an internal reference is selected, a voltage of 1.024V or 2.048 is available. The internal reference can source up to 1mA and can therefore be used as an external system reference.

SERIAL INTERFACE

INTERFACE MODES

The control interface can operate in two different modes:

- In the microcontroller mode, FS needs to be held low until all 16 data bits have been transferred. If FS is driven high before the 16th falling clock edge, the data transfer is cancelled. The DAC is updated after a rising edge on FS.
- In DSP mode, FS only needs to stay low for 20ns, and can go high before the 16th falling clock edge.

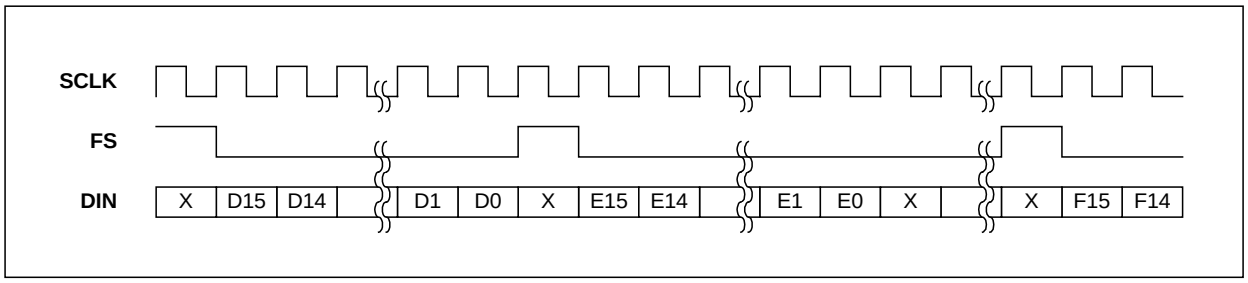


Figure 7 Interface Timing in Microcontroller Mode

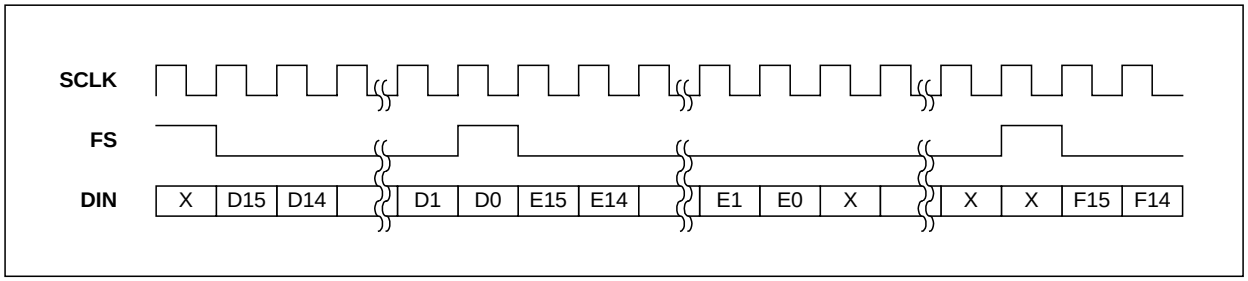


Figure 8 Interface Timing in DSP Mode

The operating mode is selected using pin 17 (MODE).

MODE PIN (17)	INTERFACE MODE
HIGH	Microcontroller
LOW or unconnected	DSP mode

Table 2 Interface Mode Selection

SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the interface timing. The maximum serial clock rate is:

$$f_{SCLK\,\max} = \frac{1}{t_{WH\,\min} + t_{WL\,\min}} = 31MHz$$

Since a data word contains 16 bits, the sample rate is limited to

$$f_{s\,\max} = \frac{1}{16(t_{WH\,\min} + t_{WL\,\min})} = 1.95MHz$$

However, the DAC settling time to 8 bits accuracy limits the response time of the analogue output for large input step transitions.

DAISY CHAINING MULTIPLE DEVICES

The DOUT output (pin 19) provides the data sampled on DIN with a delay of 16 clock cycles. This signal can be used to control another WM2632 or similar device in a daisy-chain type circuit.

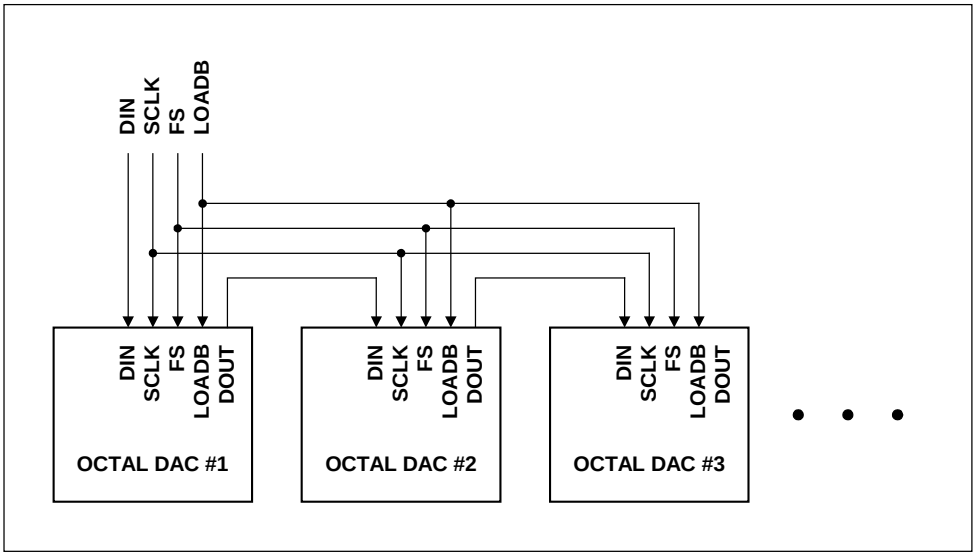


Figure 9 Daisy Chaining

SOFTWARE CONFIGURATION OPTIONS

DATA FORMAT

The WM2632 is controlled with a 16-bit code consisting of four address bits, A0-A3, and 12 data bits.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	Data											

Table 3 Input Data Format

Using the four address bits, 16 different registers can be addressed.

A3	A2	A1	A0	REGISTER
0	0	0	0	DAC A Code
0	0	0	1	DAC B Code
0	0	1	0	DAC C Code
0	0	1	1	DAC D Code
0	1	0	0	DAC E Code
0	1	0	1	DAC F Code
0	1	1	0	DAC G Code
0	1	1	1	DAC H Code
1	0	0	0	Control Register 0
1	0	0	1	Control Register 1
1	0	1	0	Preset all DACs
1	0	1	1	RESERVED
1	1	0	0	DAC A and complement B
1	1	0	1	DAC C and complement D
1	1	1	0	DAC E and complement F
1	1	1	1	DAC G and complement H

Table 4 Register Map

DAC A TO H CODE REGISTERS

Addresses 0 to 7 are the DAC registers. Bits D11 (MSB) to D4 (LSB) from these registers are transferred to the respective DAC when the LOADB input (pin 18) is low. Bits D3 to D0 are unused and must be set to 0. For instantaneous updating, LOADB can be held low permanently.

CONTROL REGISTER 0

Control register 0 (address 8) is used to select functions that apply to the whole IC, such as Power Down and Data Input Format.

BIT	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	X	PD	DO	R1	R0	IM
Default	X	X	X	X	X	X	X	0	0	0	0	0

Table 5 Control Register 0 Map

BIT	DESCRIPTION	0	1
PD	Full device Power Down	Normal	Power Down
DO	DOUT Enable	Disabled	Enabled
R1	Int / Ext Reference Select	External	Internal
R0	Internal Reference Select	1.024V	2.048V
IM	Input Mode	Straight Binary	Two's Complement
X	Reserved		

Table 6 Control Register 0 Functionality

CONTROL REGISTER 1

Control register 1 (address 9) is used to power down individual pairs of DACs and select their settling time. Powering down a pair of DACs disables their amplifiers and reduces the power consumption of the device. The settling time in fast mode is typically 1µs. In slow mode, the settling time is typically 3µs and power consumption is reduced.

BIT	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	P_{GH}	P_{EF}	P_{CD}	P_{AB}	S_{GH}	S_{EF}	S_{CD}	S_{AB}
Default	X	X	X	X	0	0	0	0	0	0	0	0

Table 7 Control Register 1 Map

BIT	DESCRIPTION	0	1
P_{XY}	Power Down DACs X and Y	Normal	Power Down
S_{XY}	Speed Setting for DACs X and Y	Slow	Fast

Table 8 Control Register 1 Functionality

DAC PRESET REGISTER

The Preset register (address 10) makes it possible to update all eight DACs at the same time. The value stored in this register becomes the digital input to all the DACs when the asynchronous PREB input (pin 5) is driven low. If no data has previously been written to the preset register, all DACs are set to zero scale.

TWO-CHANNEL REGISTERS

The two-channel registers (addresses 12 to 15) provide a 'differential output' function where writing data to one DAC will automatically write the complement to the other DAC in the pair. For example, writing a value of 255 to address 12 will set DAC A to full scale and DAC B to zero scale.

PROGRAMMABLE INTERNAL REFERENCE

The reference can be sourced internally or externally under software control. If an external reference voltage is applied to the REF pin, the device must be configured to accept this.

If an external reference is selected, the reference voltage input is buffered which makes the DAC input resistance independent of code. The REF pin has an input resistance of 10MΩ and an input capacitance of typically 55pF. The reference voltage determines the DAC full-scale output.

If an internal reference is selected, a voltage of 1.024V or 2.048 is available. The internal reference can source up to 1mA and can therefore be used as an external system reference.

REF1	REF0	REFERENCCE
0	0	External (default)
0	1	1.024V
1	0	2.048V
1	1	External

Table 9 Programmable Internal Reference

APPLICATIONS INFORMATION

LINEARITY, OFFSET, AND GAIN ERROR

Amplifiers operating from a single supply can have positive or negative voltage offsets. With a positive offset, the output voltage changes on the first code transition. However, if the offset is negative, the output voltage may not change with the first code, depending on the magnitude of the offset voltage. This is because with the most negative supply rail being ground, any attempt to drive the output amplifier below ground will clamp the output at 0 V. The output voltage then remains at zero until the input code is sufficiently high to overcome the negative offset voltage, resulting in the transfer function shown in Figure 10.

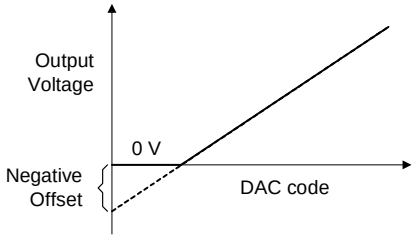


Figure 10 Effect of Negative Offset

This offset error, not the linearity error, produces the breakpoint. The transfer function would follow the dotted line if the output buffer could drive below the ground rail.

DAC linearity is measured between zero-input code (all input bits at 0) and full-scale code (all inputs at 1), disregarding offset and full-scale errors. However, due to the breakpoint in the transfer function, single supply operation does not allow for adjustment when the offset is negative. In such cases, the linearity is therefore measured between full-scale and the lowest code that produces a positive (non-zero) output voltage.

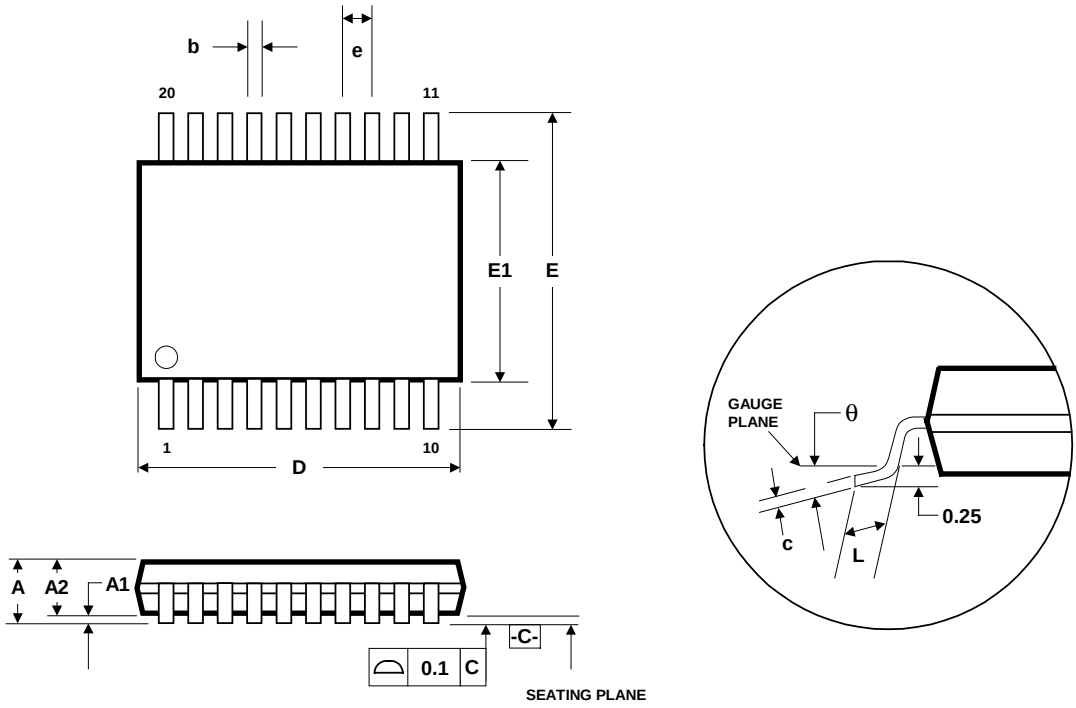
POWER SUPPLY DECOUPLING AND GROUNDING

Printed circuit boards with separate analogue and digital ground planes deliver the best system performance. The two ground planes should be connected together at the low impedance power supply source. Ground currents should be managed so as to minimise voltage drops across the ground planes.

A 0.1µF decoupling capacitor should be connected between the positive supply and ground pins of the DAC, with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analogue supply from the digital supply.

PACKAGE DIMENSIONS

DT: 20 PIN TSSOP (6.5 x 4.4 x 1.0 mm) **DM008.D**



Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	6.40	6.50	6.60
e	0.65 BSC		
E	6.4 BSC		
E_1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0^o	-----	8^o
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.