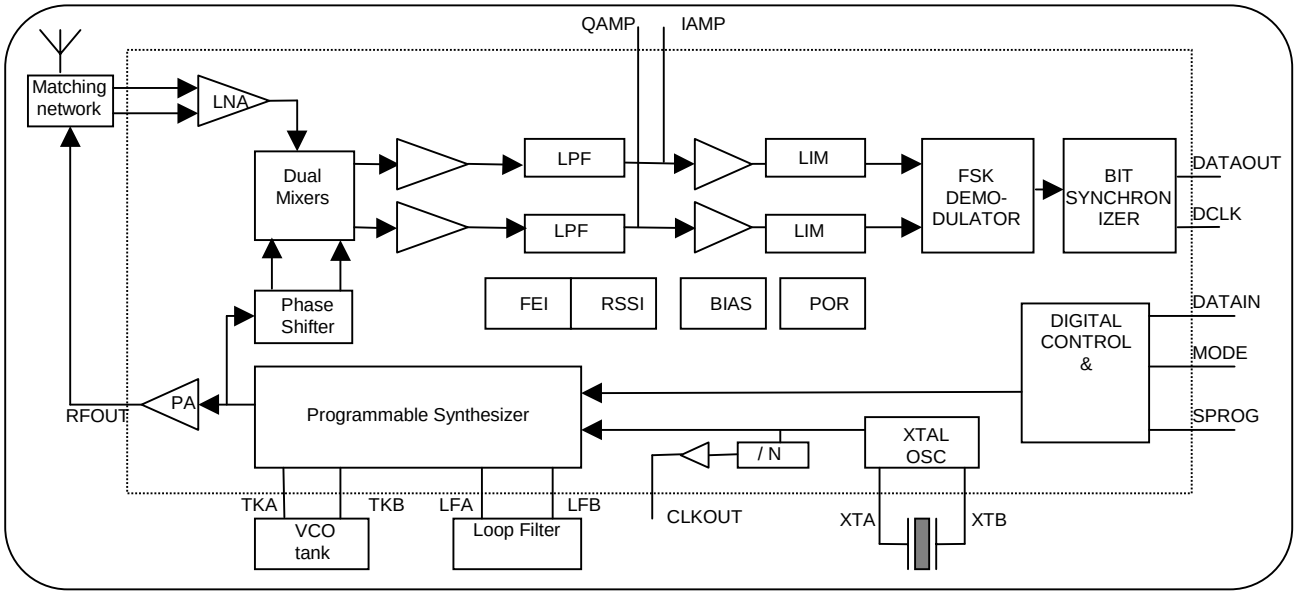
XEMICS

XE1202
Data Sheet



Preliminary Specifications:

XE1202 433 / 870 / 915 MHz

Low-Power UHF Transceiver

Features

- Low voltage operation : down to 2.7 volt
- Low-power consumption
- High sensitivity
- Frequency synthesizer by integrated PLL, covering European and US ISM bands
- Data rate up to 76.8 kbps
- Frequency deviation from 5 kHz to 100 kHz
- On-chip bit synchronizer
- Few external components
- Transmit power : up to +15 dBm
- Direct conversion architecture

Applications

- Process & Buiding Control
- Security systems
- Wireless data link
- Home appliances
- Remote control
- Wireless sensing

Ordering Information

Part	Temperature range	Pin-package
XX1202	-40 to 85° C	TQFP 44 pins

General Description

The XX1202 is a FSK one-chip transceiver circuit including both the RF front-end and the baseband processing section. It can operate in the 915 MHz, 870 MHz and 433 MHz ISM bands. The modulation used is the Frequency Shift Keying (FSK).
The LO is generated by a fully integrated frequency synthesizer allowing multi-channels operations. Different VCO tank tuning is used for configuring the circuit operation in the chosen frequency band. The FSK modulation is realized by dynamic change of the fractional-N divider ratio according to the input data stream.

Quick Reference Data

- supply voltage 2.7 V
- current consumption 12 mA (RX)
  33 mA (TX,+5dBm)
- Sensitivity -113 dBm
- data rate 76.8 kbits/s
- transmitted power +15 dBm max
- modulation CP-FSK

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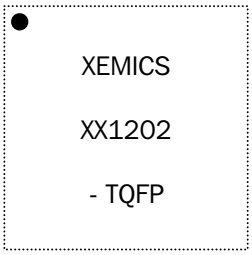
XE1202 : – 433- / 868- / 915-MHz
Low Power UHF Transceiver

Pin List

PIN	NAME		DESCRIPTION
1	MODE(1)	I/O	
2	MODE(0)	I/O	
3	EN	In	Chip Enable
4	VSS	In	GROUND
5	RFA	In	RFINPUT
6	RFB	In	RFINPUT
7	VSS	In	GROUND
8	VSS	In	GROUND
9	RFOUT	Out	RF OUTPUT
10	VDD	In	SUPPLY VOLTAGE
11	TVCO		TEST
12	VDD	In	SUPPLY VOLTAGE
13	TKA	I/O	VCO TANK
14	TKB	I/O	VCO TANK
15	VSS	In	GROUND
16	LFB	I/O	LOOP FILTER OF THE PLL
17	VDD	In	SUPPLY VOLTAGE
18	VSS	In	GROUND
19	TSUPP	In	TEST
20	LFA	I/O	LOOP FILTER OF THE PLL
21			NC
22	TMOD(0)	In	TEST BUS
23	TMOD(1)	In	TEST BUS
24	VSS	In	DROUND
25	XTA	I/O	QUARTZ AND INPUT OF EXTERNAL CLOCK
26	VSS	In	GROUND
27	XTB	I/O	QUATRZ
28	VDD	In	SUPPLY VOLTAGE
29	QAMP	Out	OUTPUT OF Q LP FILTER
30	IAMP	Out	OUTPUT OF I LP FILTER
31	TMOD(2)	In	TEST BUS
32	TMOD(3)	In	TEST BUS
33	NC		NOT CONNECTED
34	VDD	In	SUPPLY VOLTAGE
35	SO	In	SERIAL OUTPUT
36	SI	Out	SERIAL INPUT
37	SCK	I/O	SERIAL CLOCK
38	CLOCKOUT	Out	Clock out at 9.75MHz
39	VSS	In	GROUND
40	DCLK	Out	RECEIVED DATA CLOCK
41	DATAOUT	Out	RECEIVED DATA OUTPUT
42	DATAIN	In	DATA INPUT STREAM
43	NC		NOT CONNECTED
44	MODE(2)	I/O	



Absolute Ratings

- supply voltage 2.7 V to 3.6 V
- storage temperature -55°C to 125°C

XE1202 : – 433- / 868- / 915-MHz
Low Power UHF Transceiver

Electrical Characteristics

Tamb = 25° C; VDD = 3.3 V; XTAL : 39 MHz, Fo = 915 MHz, Binary FSK transmission, FDA = 5 kHz, DR=4.8 kbps, BWssb = 10 kHz, BER=0.01 unless otherwise specified)

SYMB.	PARAMETERS	CONDITIONS	Min	Typ	Max	Units
VDD	Operating supply voltage		2.7	3.3	3.6	V
TMPR	Operating temperature		-40		+85	°C
IDDoff	Supply current (power down)			0.2	1	uA
IDDst	Stabdby supply current	Quartz (39MHz) running		0.75	1	mA
IDDr	Receive supply current			12	13.5	mA
IDDt	Transmit supply current	+ 5 dBm RFout +15 dBm RFout		33 48		mA mA
RFS	RF sensitivity	A mode B mode		-113 -102	-110 -99	dBm dBm
FDA	Frequency deviation	Programmable with SPROG		5 10 20 100		kHz
CCR	Co-channel rejection		-11	-8		dBc
IP3	Input intercept point	A mode B mode	-43 -28	-40 -25		dBm dBm
ML	Maximum receiver input level				-20	dBm
BW	Base Band filter bandwidth	Programmable		10 20 40 200		kHz
ACR	Adjacent channel rejection	@ 65 kHz, Pw=-110 dBm	45	48		DBc
DR	Data rate	Programmable with SPROG		4.8 9.6 19.2 38.4 79.8 100*		kbps
RFout	RF output power	Programmable with SPROG		0 5 10 15		dBm
FR	Synthesizer frequency range		902 868 433 216		928 870 435 218	MHz
Tr	Receiver wake-up time	From PLL running		100	150	us
Tt	Transmitter wake-up time	From PLL running		100	150	us
Tpll	Frequency synthesizer start-up	From oscillator running		200	250	us
T_BB1	Receiver Base-Band wake-up time, Step 1	From oscillator running, C6=0, Mode(2:0)= 010 and 011		2	2.5	ms
T_BB2	Receiver Base-Band wake-up time, Step 2	From oscillator running, C6=0, Mode(2:0)= 100		0.30	0.35	ms
T_BB0	Receiver Base-Band wake-up time, Only one step	From oscillator running, C6=1, Mode(2:0)= 010 and 011		2.5	3.5	ms
T_RS	RSSI Wake-up time	From receiver running			1	ms
T_OS	Quartz Oscillator Wake-up time				2	ms

SYMB.	PARAMETERS	CONDITIONS	Min	Typ	Max	Units
T_FE	FEI Wake-up time	From receiver running C4=1 C4=0			20/DR 4/DR	ms
Fs	Frequency synthesizer step			500		Hz
Xtal	Crystal frequency			39		MHz
VTHR	Equivalent input thresholds of the RSSI	MODE A Low range: VTHR1 VTHR2 VTHR3 MODE B High range: VTHR1 VTHR2 VTHR3		 -105 -100 -95 -90 -85 -80		dBm
FERR	Error threshold for the FEI	Pw=-100dBm (Mode A)		0.5		
SPR	Spurious Emission in receiver mode			-63	-60	dBm
VIH	Digital input level high	In % of VDD	75			%
VIL	Digital input level low	In % of VDD			25	%
VOH	Digital output level high	In % of VDD	75			%
VOL	Digital output level low	In % of VDD			25	%

Functional Description

The XE1202 is a single-chip half-duplex data transceiver. It includes a receiver, a transmitter, a frequency synthesizer and some service blocks. The circuit operates in 4 frequency ranges (217MHz, 433MHz, 870MHz, 915MHz) and uses 2-level FSK modulation.

The XE1202 is controlled via the 3-wires serial bus by a microcontroller that addresses the 3-wires (SCK- Serial Clock, SI- Serial Input, SO – Serial Output). According to the figure 1 and 2 a bit stream of 13 bits (1 Start, 1 R/W, 3 address, 8 data) is fed into the internal registers with the Most Significant Bit (MSB) first.

In order to optimize the power consumption, the XE1202 has 7 different types of operating mode. These modes are addressed by 3 external pins; MODE(2:0).

The circuit is constituted of 5 main functional blocks:

- The receiver

The receiver converts a 2level FSK modulated signal into a bit stream. The final output are DATAOUT and DCLK, which are generated by the Bit Synchronizer; this block transforms the output bit stream of the demodulator into a glitch free bit stream and generates a synchronize clock with the data.
Besides the receiver chain itself, there are two additional blocks:

- an RSSI block (Received Signal Strength Indicator) giving the range of the received signal level at the output of the Base Band filters,
- A FEI block (Frequency Error Indicator), giving an indication about the frequency error of the local oscillator.

- The transmitter,

The transmitter performs the modulation of the carrier by an input bit stream and the transmission of the modulated signal. The modulation is made directly through the frequency synthesizer. A power amplifier whose power is programmable on four values amplifies the modulated signal. The frequency deviation and the bit rate are programmable on the same values as in the receiver; an additional pair of frequency deviation / bit rate allowing a transmission at 100kbps to be performed is also implemented.

- The Frequency synthesizer

The frequency synthesizer generates the carrier (LO) signal for the receiver and the modulated signal for the power amplifier of the transmitter. The frequency is programmable with a step of 500Hz in four frequency bands. The block includes a quartz oscillator, which provides the PLL with the reference signal.

- The service blocks

These blocks perform all the functions needed by the circuit to work properly.

- The control block

The control block is the digital circuit generating the control signals for all the sub-blocks of the XE1202 according to the configuration selected by the user.

Configuration Register

The first three bits (A10, A9, and A8) determine the B, C, D, E, F and G register access according to the truth table below.

A10	A9	A8	REGISTER NAME
0	0	0	REGISTER B
0	0	1	REGISTER C
0	1	0	REGISTER D
0	1	1	REGISTER E
1	0	0	REGISTER F
1	0	1	REGISTER G

- **"B" REGISTER FORMAT**

(A15=0, A14=0, A13=0)

A	A	A	B	B	B	B	B	B	B	B
10	9	8	7	6	5	4	3	2	1	0

✻ B7 – RECEIVER MODE

When set to 0, this bit configure the XE1202 in high sensitivity mode (MODE A). The typical value of sensitivity is –113dBm and the value of IP3 (Input interception point) is –40dBm. When it is set to 1, the XE1202 is configured in high linearity (MODE B). In this case the sensitivity's value is –102dBm and IP3 value is –25dBm.

	SENSITIVITY	IP3
B7=0 - MODE A	-113dBm	-40dBm
B7=1 - MODE B	-102dBm	-25dBm

✻ B6 – BIT SYNCHRONIZER ON/OFF

When set to 0, this bit disables the Bit Synchronizer when set to 1 the Bit Synchronizer is enable.

	BIT SYNCHRONIZER
B6=0	OFF
B6=1	ON

✻ B5 – RSSI ON/OFF

The Receiver Signal Strength Indication is switched off if B5 is set to 0. When B5 is set to 1 the RSSI is switched on. In this mode the RRSI output is given by G7 and G6.

	RRSI ON/OFF
B5=0	OFF
B5=1	ON

✻ B4 – FEI ON/OFF

The Frequency Error Indication is switched off if B4 is set to 0. When B4 is set to 1 the FEI is switched on. In this mode G5 and G4 give the FEI output.

	FEI ON/OFF
B4=0	OFF
B4=1	ON

✻ B3, B2 – BANDWIDTH OF THE BASE BAND FILTER

The bandwidth of the base band filter can be adjusted with B3 and B2 according to following table.

B3	B2	BANDWDTH
0	0	10 kHz
0	1	20 kHz
1	0	40 kHz
1	1	200 kHz

✻ B1, B0 – TRANSMITTER OUTPUT POWER

The output power available at RFOUT can be adjusted with B1 and B0 between 0dBm for the minimum and 15dBm for the maximum

B1	B0	OUTPUT POWER
0	0	0 dBm
0	1	5 dBm
1	0	10 dBm
1	1	15dBm

"C" REGISTER FORMAT

(A15=0, A14=0, A13=1)

A	A	A	C	C	C	C	C	C	C	C
10	9	8	7	6	5	4	3	2	1	0

✻ C7, C6 – TEST BITS

✻ C6 – WAKE–UP MODE OF THE BASE BAND
The XE1202 allows the receiver mode to be configured in two separate ways. When C6 is set to 0, the Base band processing is waken up in a sequence of three steps. When C6 is set to 1, the Base Band is waken up in one mode.

	WAKE-UP MODE
C6=0	Successive steps
C6=1	Only one step

✻ C5 – PRE-FILTERING
The modulation of the Local Oscillator frequency by the modulating bit stream can be made in two ways. If the bit C5 is set to 0, the input bit stream is directly applied to the frequency synthesizer without any filtering. If the C5 is set to 1, the input bit stream is pre-filtered before being applied to the frequency synthesizer; with this filtering, each edge of the bit stream is linearly smoothed with a staircase transition. In this mode the bit C3 (PARAMETER STAIR) needs to be configured.

✻ C4 – FEI SELECTION
This bit is used to select the Frequency Error Indication structure.

	WAKE-UP MODE	WAKE UP TIME
C4=0	FEI using Flip Flop Demodulator	4 / Data Rate
C4=1	FEI using correlators	20/ Data Rate

✻ C3 – PARAMETER STAIR IN TRANSMITTER MODE
The characteristic of the filtering is the ratio t_{rise} / t_{bit}. The value of this ratio is programmable on two values.

	t_{rise} / t_{bit}
C3=0	10% of bit duration
C3=1	20% of bit duration

✻ C2 – MODULATION ON/OFF
In transmitter mode, when the bit C2 is set to 0, the modulation is ON when set to 1 the modulation is OFF.

	MODULATION ON/OFF
C2=0	ON
C2=1	OFF

✻ C1 – RSSI RANGE
The XE1202 allows configuring two different ranges for the RSSI function. The low range and the high range according to the following table.

	VTH1	VTH2	VTH3
C1=0 Low range	-105dBm	-100dBm	-95dBm
C1=1 High range	-90dBm	-85dBm	-80dBm

✻ C0– TEST BITS

• "D" REGISTER FORMAT
FREQUENCY PARAMETER

(A15=0, A14=1, A13=0)

A	A	A	D	D	D	D	D	D	D	D
10	9	8	7	6	5	4	3	2	1	0

✻ D7, D6 – FREQUENCY BAND
These bits are used to select the frequency band between 4 pre-defined values.

D7	D6	FREQUENCY BAND
0	0	216 – 218 MHz
0	1	433 – 435 MHz
1	0	868 – 870 MHz
1	1	902 – 928 MHz

✻ D5, D4, D3 – FREQUENCY DEVIATION
These bits are used to select the frequency deviation between 5 pre-defined values.

D5	D4	D3	FREQUENCY DEVIATION
0	0	0	5 kHz
0	0	1	10 kHz
0	1	0	20 kHz
0	1	1	40 kHz
1	0	0	100 kHz

✻ D2, D1, D0 – BIT RATE
These bits are used to select the data rate between 6 pre-defined values.

D2	D1	D0	DATA RATE
0	0	0	4.8 kb/s
0	0	1	9.6 kb/s
0	1	0	19.2 kb/s
0	1	1	38.4 kb/s
1	0	0	76.8 kb/s
1	0	1	100 kb/s in transmitter mode

- **"E - F" REGISTERS FORMAT**

FREQUENCY PARAMETER

E = (A15=0, A14=1, A13=1)
F = (A15=1, A14=0, A13=0)

REGISTER E

A	A	A	E	E	E	E	E	E	E	E
10	9	8	7	6	5	4	3	2	1	0

REGISTER F

A	A	A	F	F	F	F	F	F	F	F
10	9	8	7	6	5	4	3	2	1	0

✻ E7-E0; F7-F0 – LOCAL OSCILLATOR FREQUENCY
The local oscillator value is given in 2's complement representation.

E7 – E0; F7- F0	Flo
00…0	Middle of the range
0X…X	Higher than the middle of the range
1X…X	Lower than the middle of the range

- **"G" REGISTERS FORMAT**

DATA OUT FORMAT

(A15=1, A14=0, A13=1)
REGISTER G

A	A	A	G	G	G	G	G	G	G	G
10	9	8	7	6	5	4	3	2	1	0

✻ G7, G6 – RSSI OUTPUT
See **RSSI Output** chapter

✻ G5, G4, G3, G2, G1, G0 – FEI OUTPUT
See **FEI Output** chapter

SERIAL INTERFACE

A microcontroller can read and write in the configuration register through the serial interface. The three wires of this interface are:

- SCK, which is the clock provided by the microcontroller.
- SI, which is the wire supporting the data going from the microcontroller to the XE1202.
- SO, which is the wire supporting the data from the XE1202 to the microcontroller.

The time diagram of a write sequence is given in figure 1. The sequence is initiated by the microcontroller, which sets the pin “SI” to 0 during a period, of “SCK”. After this start bit (bit = 0), the microcontroller sends a R/W bit indicating which operation has to be performed; this bit is set low for a write operation and high for a read operation.

The next 3 bits sent by the microcontroller are the address of the register to be accessed. The next 8 bits are the data to be written in the register. The data on “SI” must change on the rising edges of “SCK” and are sampled by the configuration register at the falling edges. The transmission is automatically closed after the 13th falling edge of “SCK” (edge during start bit taken into account), whatever happens on “SI” afterwards. The wire “SI” must go high at least once after the transmission in order to the start bit of the next transmission to be detected. The duty cycle of “SCK” must be between 40% and 60% for a maximum frequency of 1MHz.

The time diagram of a read sequence is given in figure 2. Once the address of the register has been sent by the microcontroller, the data from the XE1202 are transmitted on pin “SO”. The data on this pin are changed at the rising edges of “SCK” and must be sampled by the microcontroller at the falling edge.

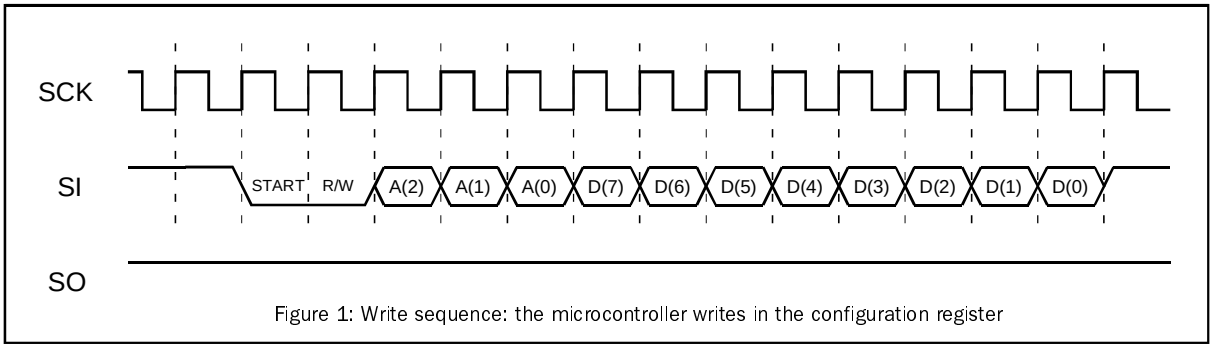


Figure 1: Write sequence: the microcontroller writes in the configuration register

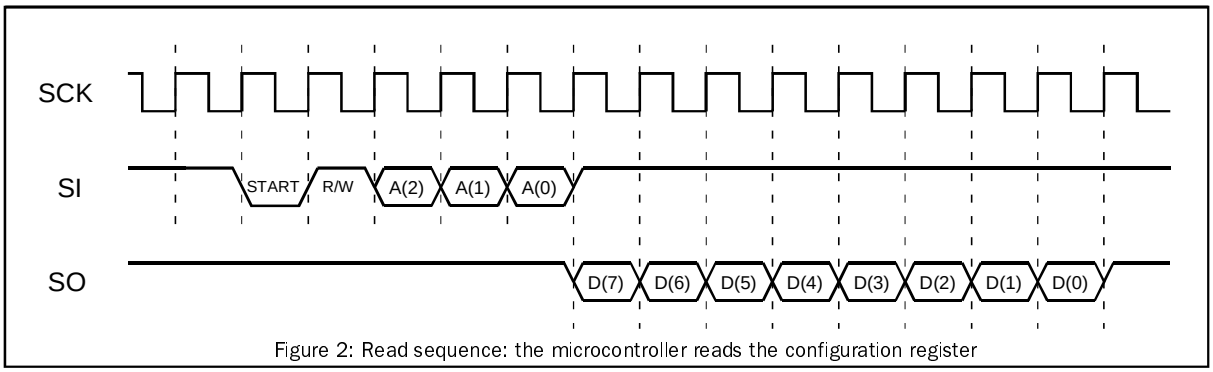


Figure 2: Read sequence: the microcontroller reads the configuration register

SYSTEM START-UP

The XE1202 contains a Power-on-Reset block which provides the digital control block with a signal used to reset the configuration registers in its default states; in this default states, all the register bits are reset to 0.

OPERATING MODES

The main operating modes of the transceiver are described in *table 1*. The chosen mode is selected through the vector MODE (2:0).

When the XE1202 is switched from the standby mode to the receiver or transmitter mode, the sub-blocks can be powered on at different times, in order to optimize the consumption of the circuit. These wake-up sequences can be organized by the microcontroller, which can configure the XE1202 in different sub-modes.

When the value of MODE (2:0) is changed, the switching from the previous mode to the new one is made on the rising edge of EN pin.

WAKE-UP MODES

Three different ways of Base Band processing waking-up are implemented and can be selected with the bit register C6.

When C6 is set to low, the Base Band processing block is waken-up in a sequence of three steps.

1. Mode (2:0) = 010 then 011. The Base Band processing is woken up, but its input is disconnected from the output of the RF front-end of the receiver.
2. Mode (2:0) = 100. The RF front-end is woken up first. To accelerate the wake up cycle, the input of the base-band block is temporarily connected to the RF Front end receiver. A current is then injected to the block whose function is to compensate the output of the RF front-end output set.
3. Mode (2:0) = 101. The additional current in the Base Band filter is cut off and the Base band-processing block enters its normal working mode.

When the bit C6 is set high, the Base band processing block is woken up in one step, which means that it is directly connected to the output of the RF front end of the receiver and no additional current in injected mode when Mode (2:0) = 100. In this case the Mode (2:0) =101 is not used. The time duration when the RF front end, the frequency synthesizer and the Base band processing block have to be awake together before a right reception can be done is much longer than in the first mode where the bit C6 is set to low.

TRANSMITTER FUNCTION

The input bit stream DATAIN for the transmitter can be connected directly to a microcontroller.

RECEIVER FUNCTION

The outputs of the receiver are the two signals DATAOUT and DCLK. When the bit B6=1, the Bit Synchronizer is on and the two output signals are respectively the output bit stream and the synchronize clock. The function of the bit synchronizer is to remove the glitches from the bit stream DATAOUT and to provide the output clock DCLK. The value of DATAOUT is valid at the rising edge of DCLK.

For a proper behavior of the Bit Synchronizer, three conditions have to be satisfied:

- a preamble of 20 bits is required for the synchronization; this preamble must be a sequence of 0 and 1 sent alternatively
- during transmission of data, the bit stream must have at least one transmission form 0 to 1 or from 1 to 0 every 8 bits,
- the accuracy of the bit rater must be better than ±5%.

When the bit B6 is low, the Bit Synchronizer is off and the signal DATAOUT is the output of the demodulator; in this case, DCLK is not used.

NAME	MODE (2:0)	RUNNING SUB-BLOCKS OF THE RECEIVER
Sleep Mode	000	-
Standby Mode	001	Quartz Oscillator
Receiver Mode	010	Quartz oscillator, Base Band processing
	011	Quartz oscillator, Frequency Synthesizer, Base Band Receiver processing
	100	Quartz oscillator, Frequency Synthesizer, Full Receiver (RF front included)
	101	Submode only used when the bit C6=0: same as submode 100, but the additional current injected in the Base band filter is cut off.
Transmitter Mode	110	Quartz oscillator, Frequency Synthesizer
	111	Quartz oscillator, Frequency Synthesizer, Full Transmitter(Power amplifier included)

Table 1: Operating Mode description

The figures 3, 4, 5 give examples of the receiver and transmitter sequences.

Receiver Mode

Wake-up time mode of the Base band (C6 register)= 0

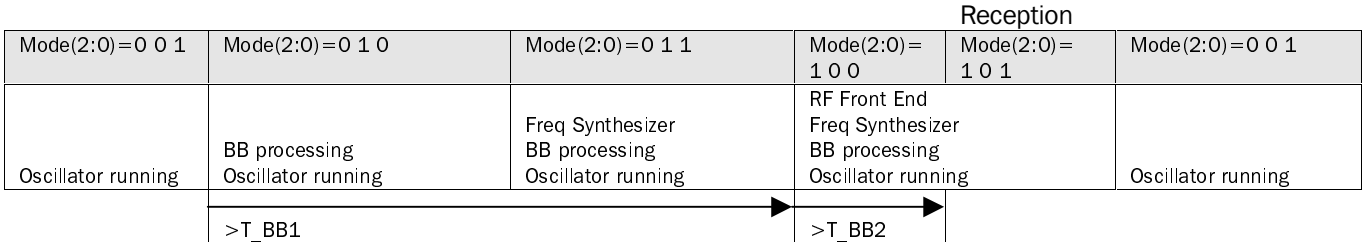


Figure 3: Receiver Sequence

Wake-up time mode of the Base band (C6 register)= 1

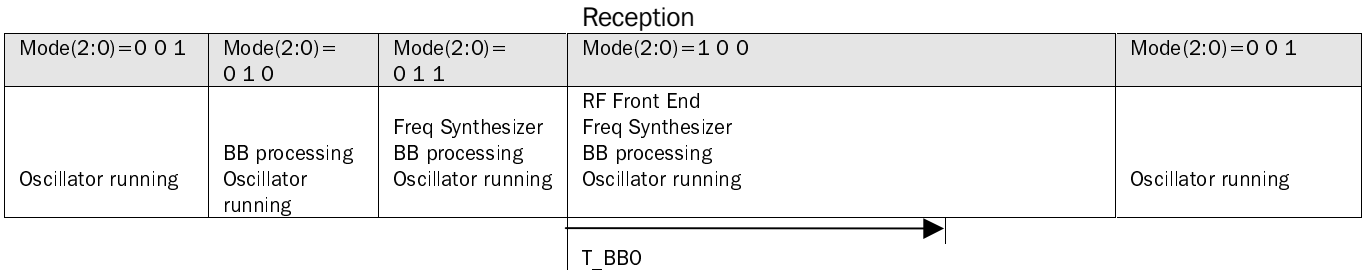


Figure 4: Receiver Sequence

Transmitter Mode

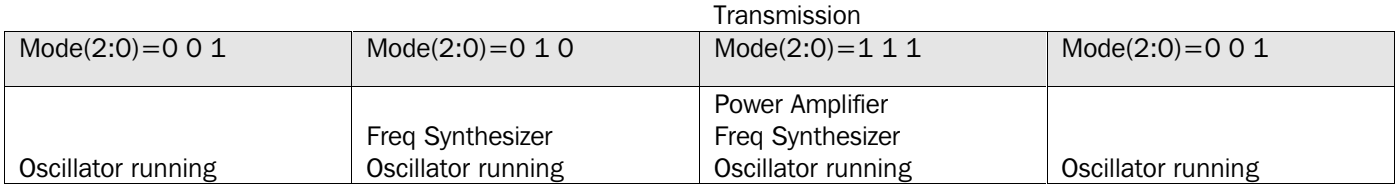


Figure 5: Transmitter Sequences

RSSI OUTPUT

This function gives a Received Signal Strength Indication obtained by measuring the signal at the output of the Base-Band filter. To active this block the register B5 must be set high. When activated, the RSSI function gives a 2-bits output that is stored in register G7 and G6. The meaning of this output is given in the following table where VRF is the differential amplitude of the equivalent input RF signal in mode A. Thus, the thresholds VTHRi given in the table correspond to mode A. These thresholds are thresholds at the output of the base-band filter divided by the gain between the input of the receiver and the RSSI output. The time diagram of RRSI measurement is given figure 6.

RSSI	OUTPUT	Meaning
G7	G6	
0	0	VRF ≤ VTHR1
0	1	VTHR1 ≤ VRF ≤ VTHR2
1	0	VTHR2 ≤ VRF ≤ VTHR3
1	1	VTHR3 ≤ VRF

Two ranges with three VTHRi are defined and selected with the register C1 (RSSI range).

The time diagram of an RSSI measurement is given in figure 6. When the RRSI block has been woken up and is ready, as long as the block is kept on, the signal strength is periodically measured and the current result of the measurement is loaded in the register G7 and G6 at each front edge of “DataIn”. The time TS_RS is the time required for the first evaluation to be completed after the function has been started up and its value is given in the Electrical performances table.

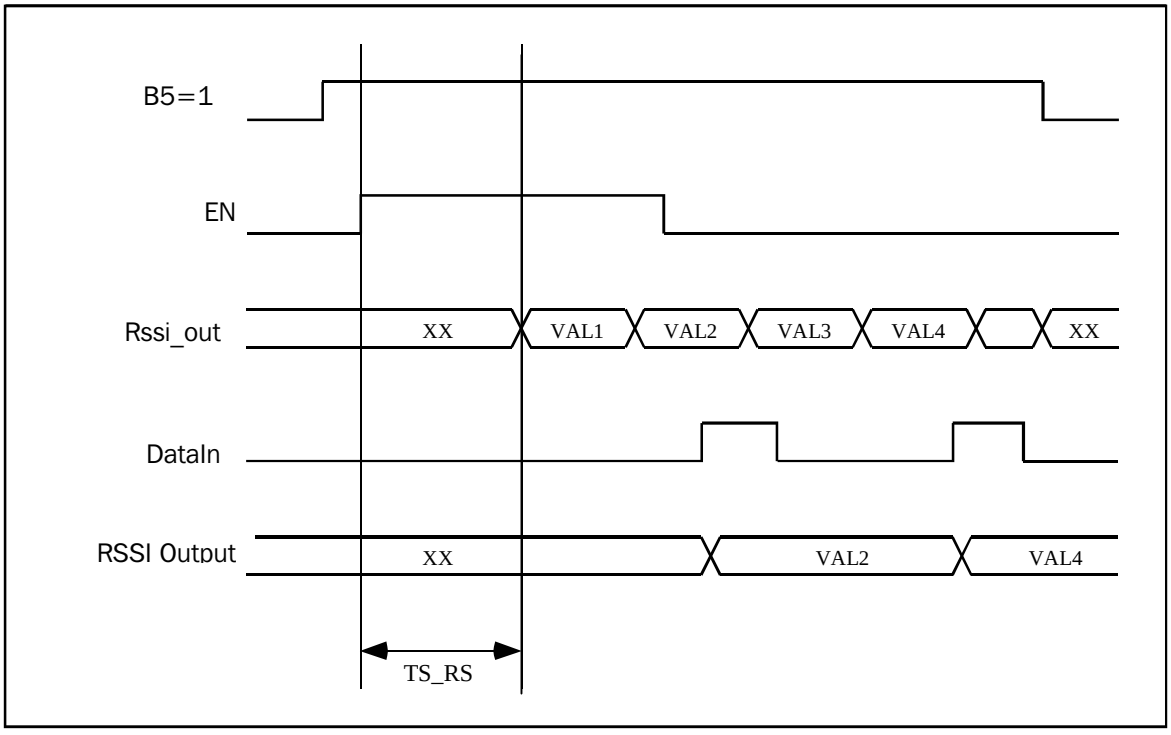


Figure 6. Time diagram of an RSSI measurement

FEI OUTPUT

C4=1
FEI using correlators

When the FEI function is activated, the output value is stored in register G5 and G4. The meaning of this output is given in the following table, where fLO is the internal Local Oscillator frequency, and the fRF is the carrier frequency of the received signal.

FEI	OUTPUT	Meaning
G5	G4	
0	0	$\lvert fLO - fRF \rvert \leq fERR$
0	1	-
1	0	$(fLO - fRF) < -fERR$
1	1	$(fLO - fRF) \geq fERR$

The threshold fERR is given by: fERR = FERR * BR

Where BR is the Bit Rate and FERR is a ratio given in the Electrical Specification table.

As Example:
For a Bit Rate of 4.8 kbps and with FERR=0.5, the fERR is 2.4 kHz.

The time diagram of an FEI is given in figure 7. When the FEI block has been woken up and is ready, the frequency error is periodically measured and the current result of the measurement is loaded in the register G5 and G4 at each rising edge of DataIn.
The latter is mainly devoted to the input bit stream of the transmitter, but is used for this FEI purpose during the receiver mode. TS_FE is the time required for the first evaluation to be completed after the block has been started up and its value is given in Electrical Specification table.

The FEI works properly if the input signal is the preamble defined in section “Receiver Function“ and if the error to be detected is lower than 20kHz

Since the contents of the configuration register are validated at the rising edge of the enable signal “EN”, the FEI block is actually started up at this time.

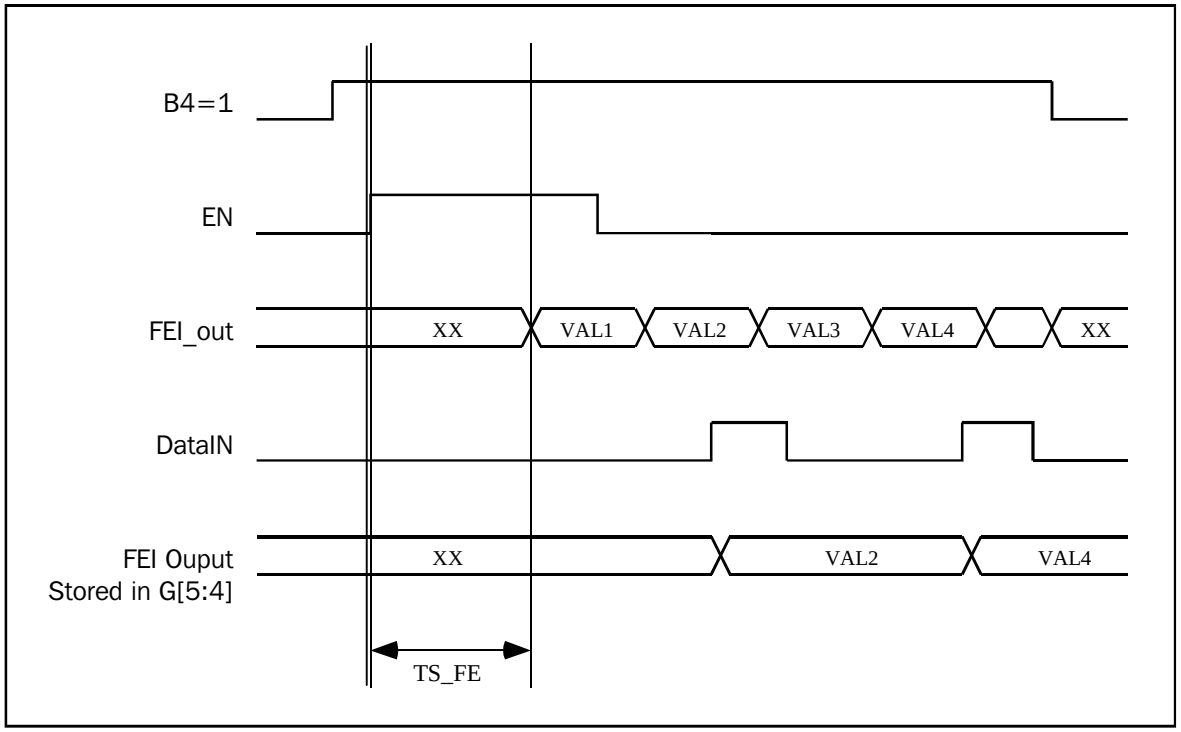


Figure 7. Time diagram of an FEI measurement when C4=1

C4=0
FEI using Flip Flop D demodulator

When activated by the signal "DataIn", the FEI block gives an 8-bits output, which is stored in register G[7:0]. This output is an output of an up/down counter, which is clocked at a frequency equal to 32 times bit the data rate. The input of this counter is the output signal of an additional FFD demodulator.

The time diagram of an FEI measurement is given in figure 8. The FEI block is woken up at the rising edge of "EN" after the register B4 has been set high through the serial interface. When the FEI has been woken up and ready (after less than 50ns), the counter is activated at the rising edge of "DataIn". Normally "DataIn" is mainly devoted to the input bit stream of the transmitter, but is used for this FEI purpose during the receiver mode. After a duration equal to TS_FE, the counter is stopped and its content is stored in the register G[7:0]. The actual delay between the rising edge of "DataIn" and the moment when the counter starts counting is lower than (1/16DR), where DR is the bit rate.

The FEI works properly if the input signal is the preamble defined in section Receiver function and if the error to be detected is lower than 20kHz.

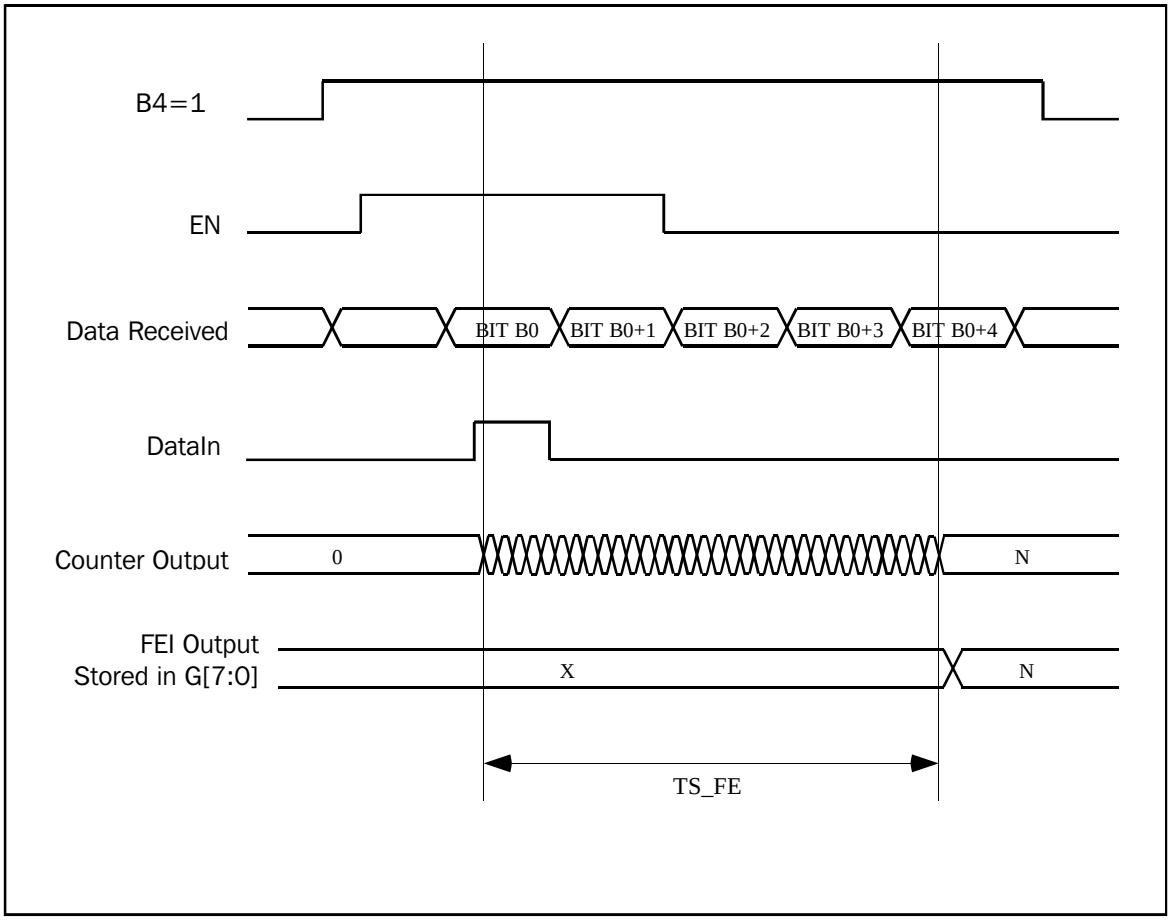
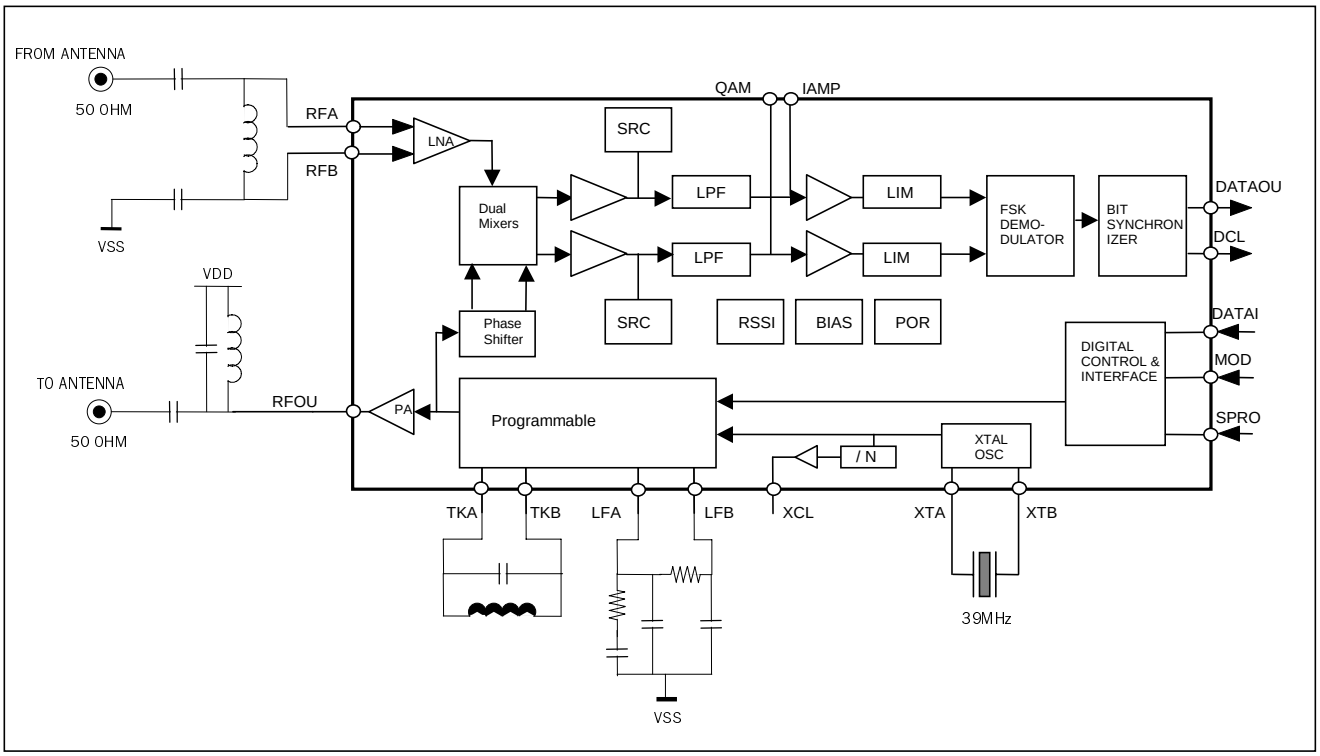


Figure 8: Timing Diagram if an FEI measurement when C4=0

XE1202 : – 433- / 868- / 915-MHz
Low Power UHF Transceiver

APPLICATION SCHEMATIC



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