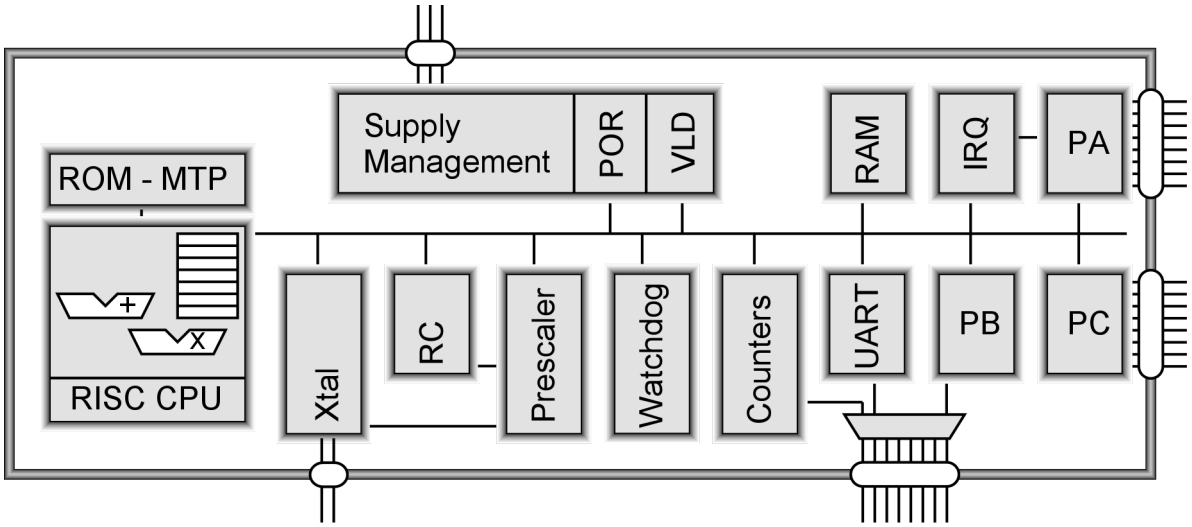


XE88LC03

Ultra Low-Power Low-Voltage Microcontroller

General Description

The XE88LC03 is an ultra low-power low-voltage microcontroller unit (MCU) with extremely high efficiency, allowing for 1 MIPS at 300uA at 2.4 V, and 8 x 8 bits multiplying in one clock cycle.

XE88LC03 is available with on chip Multiple-Time-Programmable (MTP) program memory.

Applications

- Internet connected appliances
- Portable, battery operated instruments
- RF system supervisor
- Remote control
- HVAC control

Key product Features

- Ultra low-power MCU
  - 300 uA at 1 MIPS operation
  - 6 uA at 32 kHz operation
  - 1 uA time keeping
- Low-voltage operation (2.4 - 5.5 V supply voltage)
- 22 kB (8 kW) MTP, 512 B RAM
- 4 counters
- PWM
- UART
- Analog matrix switching
- independant RC and crystal oscillators
- 5 reset, 15 interrupt, 8 event sources

Ordering Information

Nomenclature: (**XX** identifies pre-production products)

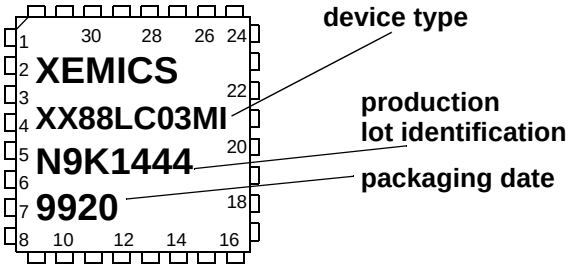
XE88LC03ME012

- program memory: M: MTP
- temperature: I: -40 to 85 °C
- package: 015: SO28, 026: TQFP32

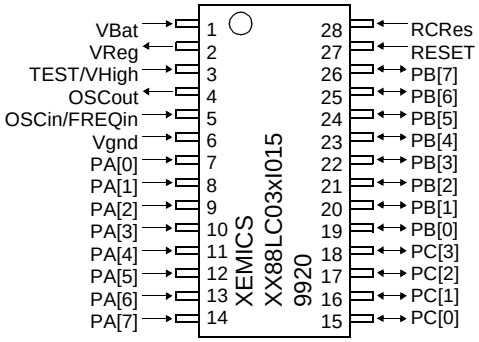
XEMICS SA, Switzerland. Tel: +41 32 720 51 70 Fax: +41 32 720 57 70 e-mail: info@xemics.com web: www.xemics.com

Low-Power Microcontroller
XX-XE88LC01

Detailed Pin Description



Pinout of the XX-XE88LC03 in TQFP32 package



Pinout of the XX-XE88LC03 in SOP28 package

Pin					Description
Position in SO28	Position in TQFP32	Function name	Second function name	Type	
1	13	Vbat		Power	Positive power supply
2	14	Vreg		Analog	Regulated supply
3	15	TEST/Vhigh	Vhigh	Special	Test mode/High voltage for MTP programing
4	16	OscOut	ptck	Analog/Input	Connection to Xtal/ Peripheral clock for test and MTP programing
5	17	OscIn	ck_cr	Analog/Input	Connection to Xtal/ CoolRISC clock for test and MTP programing
6	18	Vss		Power	Negative power supply, connected to substrate
7	19	PA(0)	testin	Input	Input of Port A/ Data input for test and MTP programing/ Counter A input
8	20	PA(1)	testck	Input	Input of Port A/ Data clock for test and MTP programing/ Counter B input
9	21	PA(2)		Input	Input of Port A/ Counter C input/ Counter capture input
10	22	PA(3)		Input	Input of Port A/ Counter D input/ Counter capture input
11	23	PA(4)		Input	Input of Port A
12	24	PA(5)		Input	Input of Port A
13	25	PA(6)		Input	Input of Port A
14	26	PA(7)		Input	Input of Port A
15	27	PC(0)		Input/Output	Input-Output of Port C
16	28	PC(1)		Input/Output	Input-Output of Port C
17	29	PC(2)		Input/Output	Input-Output of Port C
18	30	PC(3)		Input/Output	Input-Output of Port C
	31	PC(4)		Input/Output	Input-Output of Port C
	32	PC(5)		Input/Output	Input-Output of Port C
	1	PC(6)		Input/Output	Input-Output of Port C
	2	PC(7)		Input/Output	Input-Output of Port C
19	3	PB(0)	testout	Input/Output/Analog	Input-Output-Analog of Port B/ Data output for test and MTP programing/ PWM output
20	4	PB(1)		Input/Output/Analog	Input-Output-Analog of Port B/ PWM output

Pin-out of the XX-XE88LC03 in SO28 and TQFP32

Pin					Description
Position in SO28	Position in TQFP32	Function name	Second function name	Type	
21	5	PB(2)		Input/Output/Analog	Input-Output-Analog of Port B
22	6	PB(3)	SOU	Input/Output/Analog	Input-Output-Analog of Port B, Output pin of USRT
23	7	PB(4)	SCL	Input/Output/Analog	Input-Output-Analog of Port B/ Clock pin of USRT
24	8	PB(5)	SIN	Input/Output/Analog	Input-Output-Analog of Port B/ Data input or input-output pin of USRT
25	9	PB(6)	Tx	Input/Output/Analog	Input-Output-Analog of Port B/ Emission pin of UART
26	10	PB(7)	Rx	Input/Output/Analog	Input-Output-Analog of Port B/ Reception pin of UART
27	11	RESET		Input	Reset pin (active high)
28	12	RCRes		Analog	Optional external resistor for RC oscillator

Pin-out of the XX-XE88LC03 in SO28 and TQFP32

XE88LC03xI Electrical Characteristics

Operation conditions		min	typ	max	Unit	Remarks
Power supply						
		2.4		5.5	V	1
Current requirement	CPU running at 1 MIPS			310	uA	1
	CPU running at 32 kHz on Xtal, RC off			10	uA	1
	CPU halt, timer on Xtal, RC off			1	uA	1
	CPU halt, timer on Xtal, RC ready			1.7	uA	1
	CPU halt, Xtal off timer on RC at 100 kHz			1.4	uA	1
	Voltage level detection			15	uA	1
MTP	Prog. voltage	10.3		10.8	V	
	Erase time		3	30	s	
	Write/Erase cycles	10	100			
	Data retention	10			year	

Current requirement of the XE88LC03

Note: 1)Power supply: 2.4 V - 5.5 V, at 27°C; min voltage of XX version may be higher.

CPU

The XE88LC03 CPU is a low power RISC core. It has 16 internal registers for efficient implementation of the C compiler. Its instruction set is made of 35 generic instructions, all coded on 22 bits, with 8 addressing modes. All instruc-

tions are executed in one clock cycle, including conditional jumps and 8x8 multiplication, therefore the XE88LC03 runs at 1 MIPS on a 1 MHz clock.

A complete tool suite for development is available from XEMICS, including programmer, C-compiler, assembler, simulator, linker, all integrated in a modern and efficient graphical user interface.

NAME	Parameters	res	op1	op2	FUNCTION	MODIF.
JUMP	addr:16				PC0 <- addr	- , - , - , -
	ip				PC0 <- ip	
Jcc	addr:16				if cc then PC0 <- addr	
	ip				if cc then PC0 <- ip	
CALL	addr:16				PCn <- PCn-1 (n>1), PC1 <- PC0+1, PC0 <- addr	
	ip				PCn <- PCn-1 (n>1), PC1 <- PC0+1, PC0 <- ip	
CALLS	addr:16				ip <- PC0+1, PC0 <- addr:16	
	ip				ip <- PC0+1, PC0 <- ip	
RET					PCn-1 (n>0) <- PCn	- , - , - , -
RETS					PC0 <- ip	
RETI					PCn-1 (n>0) <- PCn, GIE <- 1	
PUSH					PCn <- PCn-1 (n>1), PC1 <- ip, PC0 <- PC0+1	
POP					ip <- PC1, PCn-1 (n>1) <- PCn, PC0 <- PC0+1	
MOVE	reg, data:8	reg	data		res <- op1	- , - , Z , a
	reg1, reg2	reg1	reg2			
	reg, eaddr	reg	eaddr			
	eaddr, reg	eaddr	reg			- , - , - , -
	addr:8, data:8	addr	data			
CMVD	reg1, reg2	reg1	reg2		if C=0 then res <- op1	- , - , Z , a
CMVS	reg, eaddr	reg	eaddr		if C=1 then res <- op1	
SHL	reg1, reg2	reg1	reg2		res(bitn) <- op1(bitn-1) (0<n<8), res(0) <- 0, C <- op1(7)	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
SHLC	reg1, reg2	reg1	reg2		res(bitn) <- op1(bitn-1) (0<n<8), res(0) <- C, C <- op1(7)	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
SHR	reg1, reg2	reg1	reg2		res(bitn-1) <- op1(bitn) (0<n<8), res(7) <- 0, C <- op1(0)	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
SHRC	reg1, reg2	reg1	reg2		res(bitn-1) <- op1(bitn) (0<n<8), res(7) <- C, C <- op1(0)	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
SHRA	reg1, reg2	reg1	reg2		res(bitn-1) <- op1(bitn) (0<n<8), res(7) <- op1(7), C <- op1(0)	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
CPL1	reg1, reg2	reg1	reg2		res <- NOT (op1)	-, -, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
CPL2	reg1, reg2	reg1	reg2		res <- NOT (op1) +1, if op1 = 0 then C = 1	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
CPL2C	reg1, reg2	reg1	reg2		res <- NOT (op1) +C, if op1 = 0 then C = 1	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
INC	reg1, reg2	reg1	reg2		res <- op1 +1, if overflow then C = 1	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
INCC	reg1, reg2	reg1	reg2		res <- op1 +C, if overflow then C = 1	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			

Table 1.2: XE8000 Instruction Set

NAME	Parameters	res	op1	op2	FUNCTION	MODIF.
DEC	reg1, reg2	reg1	reg2		res <- op1 -1, if underflow then C = 0	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
DECC	reg1, reg2	reg1	reg2		res <- op1 -(1 -C), if underflow then C = 0	C, V, Z, a
	reg	reg	reg			
	reg, eaddr	reg	eaddr			
AND	reg, data:8	reg	reg	data	res <- op1 AND op2	-, -, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
OR	reg, data:8	reg	reg	data	res <- op1 OR op2	-, -, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
XOR	reg, data:8	reg	reg	data	res <- op1 XOR op2	-, -, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
ADD	reg, data:8	reg	reg	data	res <- op1 + op2, if overflow then C=1	C, V, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
ADDC	reg, data:8	reg	reg	data	res <- op1 + op2 + C, if overflow then C=1	C, V, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
SUBD	reg, data:8	reg	reg	data	res <- op1 -op2, if underflow then C=0	C, V, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
SUBDC	reg, data:8	reg	reg	data	res <- op1 -op2 - (1-C), if underflow then C=0	C, V, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
SUBS	reg, data:8	reg	reg	data	res <- op2 -op1, if underflow then C=0	C, V, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
SUBSC	reg, data:8	reg	reg	data	res <- op2 -op1 - (1-C), if underflow then C=0	C, V, Z, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
MUL	reg, data:8	reg	reg	data	res <- op1 * op2 (15:8), a <- op1 * op2 (7:0), unsigned	-, -, -, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
MULA	reg, data:8	reg	reg	data	res <- op1 * op2 (15:8), a <- op1 * op2 (7:0), signed (2 complement)	-, -, -, a
	reg1, reg2, reg3	reg1	reg2	reg3		
	reg1, reg2	reg1	reg2	reg1		
	reg	reg	reg	eaddr		
MSHL	reg, shift:3				a(bitn) <- reg(bitn-shift) for (bitn >= shift), reg(bitn) <- reg (bitn+8-shift) for (bitn < shift)	-, -, -, a
MSHR	reg, shift:3				reg(bitn) <- reg(bitn+shift) for (bitn + shift < 8), a(bitn) <- reg (bitn-8+shift) for (bitn + shift >= 8)	-, -, -, a
MSHRA	reg, shift:3				a <- SHRA(shift,reg), a <- SHL(8-shift,reg), SHRA propagates sign, do not use with shift=0x01	-, -, -, a
CMP	reg, data:8		reg	data	if op2 > op1 then C <- 0, V = C AND NOT(Z), unsigned	C, V, Z, a
	reg1, reg2		reg1	reg2		
	reg, eaddr		reg	eaddr		

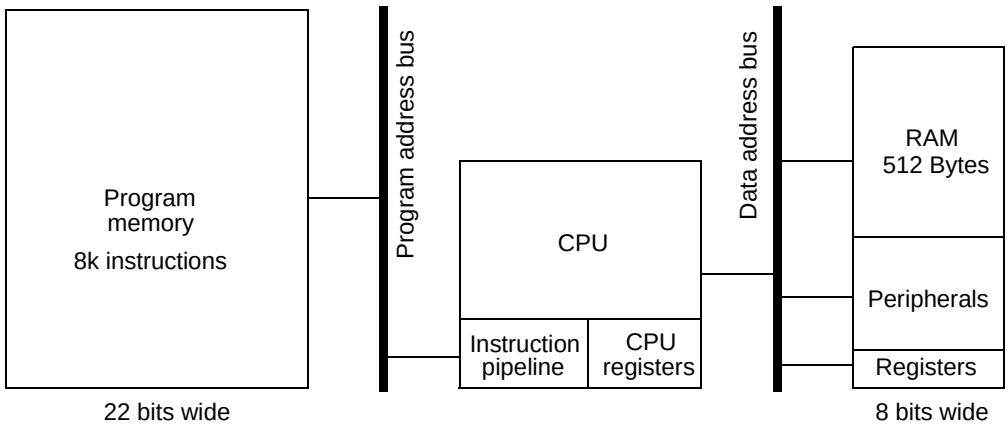
Table 1.2: XE8000 Instruction Set

NAME	Parameters	res	op1	op2	FUNCTION	MODIF.
CMPA	reg, data:8		reg	data	if op2 > op1 then C <- 0, V = C AND NOT(Z), signed	C, V, Z, a
	reg1, reg2		reg1	reg2		
	reg, eaddr		reg	eaddr		
TSTB	reg, bit:3				Z <- NOT(reg(bit))	-, -, Z, a
SETB	reg, bit:3				reg(bit) <- 1	-, -, Z, a
CLRB	reg, bit:3				reg(bit) <- 0	-, -, Z, a
INVB	reg, bit:3				reg(bit) <- NOT(reg(bit))	-, -, Z, a
SFLAG					a(7) <- C, a(6) <- C XOR V	-, -, -, a
RFLAG	reg		reg		flags <- op1, SHL op1, SHL a	C, V, Z, a
	eaddr		eaddr			
FREQ	divn:4				set cpu frequency divider	-, -, -, -
HALT					stops CPU	-, -, -, -
NOP					no operation	-, -, -, -
PMD	s:1				if s=1 then starts program dump, if s=0 stops program dump	-, -, -, -

Table 1.2: XE8000 Instruction Set

Memory organisation

The CPU uses a Harvard architecture, so that memory is organised in two separated fields: program memory and data memory. As both memory are separated, the central processing unit can read/write data at the same time it loads an instruction. Peripherals and system control registers are mapped on data memory space. Program memory is made in one page. Data is made of several 256 bytes pages.



Memory organization

Program memory

The program memory is implemented as Multiple Time Programmable (MTP) Flash memory. The power consumption of MTP is linear with the access frequency (no static current).

Memory sizes:

- Flash MTP: 8192 x 22 bits (= 22 kBytes)

block	size	address
MTP	8192 x 22	H0000 - H1FFF

Program addresses

Data memory

The data memory is implemented as static Random-Access Memory (RAM). The size is 512 x 8 bits plus 8 low power RAM bytes that require very low current when addressed, programs using this low power RAM instead of regular RAM will spare even more current.

Note: The registers in Data memory are not related to the CPU registers.

block	size	address
LP RAM	8 x 8	H0000 - H0007
RAM	512 x 8	H0080 - H027F

RAM addresses

Peripherals mapping

block	size	address	Page
LP RAM	8x8	H0000-H0007	Page 0
System control	16x8	H0010-H001F	
Port A	8x8	H0020-H0027	
Port B	8x8	H0028-H002F	
Port C	4x8	H0030-H0033	
Port D	4x8	H0034-H0037	
MTP	4x8	H0038-H003B	
Event	4x8	H003C-H003F	
Interrupts control	8x8	H0040-H0047	
reserved	8x8	H0048-H004F	
UART	8x8	H0050-H0057	
Counters	8x8	H0058-H005F	
reserved	8x8	H0060-H0067	
reserved	12x8	H0068-H0073	
reserved	8x8	H0074-H007B	
Other (VLD)	4x8	H007C-H007F	
RAM1	128x8	H0080 - H00FF	
RAM2	256x8	H0100 - H01FF	Page 1
RAM3	128x8	H0200 - H027F	Page 2

Peripherals addresses

Peripherals

The XE88LC03 includes usual microcontroller peripherals and some other blocks more specific to low-voltage or mixed-signal operation. They are 3 parallel ports, one input port (A), one IO and analog port (B) with analog switching capabilities and one general purpose IO port (C). A watchdog is available, connected to a prescaler. Four 8-bit counters, with capture, PWM and chaining capabilities are available. The UART can handle transmission speeds as high as 38kbaud.

Low-power low-voltage blocks include a voltage level detector, two oscillators (one internal 0.1-4 MHz RC oscillator and a 32 kHz crystal oscillator) and a specific regulation scheme that largely uncouples current requirement from external power supply (usual CMOS ASICs require much more current at 5.5 V than they need at 2.4 V. This is not the case for the XE88LC03).

Low-Power Microcontroller
XX-XE88LC01

XE8000 Family

Features

The main characteristics of the XE8000 MCU family is

- Ultra low power operation
- Low voltage operation (1.2 V for the XE88LC04, XE88LC06 and XE88LC07, 2.4 V for the others)
- High efficiency CPU
  - 1 instruction per clock cycle, for all instructions
  - 22 bits wide instructions
  - Integrated 8x8 -> 16 bits multiplier
  - All instructions on one page
  - 8 bits data bus
  - 8 addressing modes
- MTP (multiple time programmable) memory available
- Dual clock (X-tal and/or RC)
- Each peripheral can be set on/off individually for minimal power consumption
- UART
- Watch dog
- 4x8 bits timers with PWM ability
- Advanced acquisition path
  - Fully differential analog signal path on signal and reference
  - 4x2 or 7x1 + 1 signal input
  - 2x2 reference input
  - 0.5 - 1000 programmable gain amplifier
  - Offset programmed over +- 10 full scale
  - 5 - 16 bits resolution ADC
  - Low speed modes with reduced bias current for minimal power consumption
- Bias and signal DACs for resistive bridge sensing and analog output
- Complete development tools using Windows95 or NT graphical interface
  - Assembler
  - ANSI-C compiler
  - Source level debugger
  - Current and memory usage monitoring (Profiler)
  - CPU Simulator
  - Programmer and starter kit (XE88LC03ProStart)

Family

The XE8000 Family ultra low-power microcontroller is made of several members, all using the same microprocessor core and differing by the peripherals available.

The XE88LC01 is a low power sensing microcontroller, based on the XE88LC03, with an advanced acquisition path including differential programmable gain amplifiers and a high resolution analog to digital converter. Its main applications are dataloggers and process control.

The XE88LC02 is a low power sensing microcontroller, based on the XE88LC06 with the analog part of the XE88LC01, with an additional LCD driver. Its main applications are metering and dataloggers.

TThe XE88LC03 is a low power, low voltage, general purpose microcontroller. Its main points are the very efficient CoolRISC core, the low voltage function and the real time clock. Its main applications are low voltage control and supervision.

Low-Power Microcontroller
XX-XE88LC01

The XE88LC04 is a low power, low voltage, general purpose microcontroller, based on the XE88LC06, with an additional LCD driver. Its main points are the very efficient CoolRISC core, the low voltage function and the real time clock. Its main applications are low voltage control and supervision.

The XE88LC05 is a low power sensing microcontroller, based on the XE88LC01, with analog outputs. Its main applications are piezoresistive sensors and 4 - 20 mA loops systems.

The XE88LC06 is an improved XE88LC03, with 4 low power analog comparators. Its main applications are low voltage control and supervision.

The XE88LC07 is a smaller and even lower power microcontroller, based on the XE88LC06, with less memory.

	XE88LC01	XE88LC02	XE88LC03	XE88LC04	XE88LC05
Supply voltage	2.4 - 5.5 V	2.4 - 5.5 V	2.4 - 5.5 V	1.2- 5.5 V for ROM 2.4 - 5.5 V for MTP	2.4 - 5.5 V
Max speed	2 MIPS	4 MIPS	2 MIPS	4 MIPS at 2.4 V	2 MIPS
Operating temperature	-40 - 85 °C	-40 - 85 °C -40 - 125 °C	-40 - 85 °C	-40 - 85 °C -40 - 125 °C	-40 - 85 °C
CPU	CoolRISC 816, 22 bits instructions 8 bits data HW multiplier	CoolRISC 816, 22 bits instructions 8 bits data HW multiplier	CoolRISC 816, 22 bits instructions 8 bits data HW multiplier	CoolRISC 816, 22 bits instructions 8 bits data HW multiplier	CoolRISC 816, 22 bits instructions 8 bits data HW multiplier
Program memory	8k Instructions = 22 kB ROM or MTP	8k Instruction = 22 kB ROM or MTP	8k Instructions = 22 kB ROM or MTP	8k Instructions = 22 kB ROM or MTP	8k Instructions = 22 kB ROM or MTP
Data memory	512 + 8 Bytes	768 + 8 Bytes	512 + 8 Bytes	768 + 8 Bytes	512 + 8 Bytes
Port A	8 input and external interrupt	8 input and external interrupt	8 input and external interrupt	8 input and external interrupt	8 input and external interrupt
Port B	8 input/output and analog	8 input/output and analog	8 input/output and analog	8 input/output and analog	8 input/output and analog
Port C	8 input/output	8 input/output	4 to 8 input/output	4 to 8 input/output	8 input/output
Watchdog timer	yes	yes	yes	yes	yes
General purpose timers with PWM	4 x 8 bits	4 x 8 bits	4 x 8 bits	4 x 8 bits	4 x 8 bits
UART	yes	yes	yes	yes	yes
2-3 wires serial interface	transition detection + software	transition detection + software	transition detection + software	transition detection + software	transition detection + software
Voltage level detector	yes	yes	yes	yes	yes
Oscillators	32 kHz quartz, internal RC	32 kHz quartz, internal RC	32 kHz quartz, internal RC	32 kHz quartz, internal RC	32 kHz quartz, internal RC
LCD drivers		120 segments		120 segments	
Analog mux	Port B and 4x2 or 7x1+1	Port B and 4x2 or 7x1+1	Port B	Port B	Port B and 4x2 or 7x1+1
LP comparators		4		4	
PGA	gain 0.5 - 1000	gain 0.5 - 1000			gain 0.5 - 1000
ADC	5 - 16 bits resolution	5 - 16 bits resolution			5 - 16 bits resolution
DAC	PWM	PWM	PWM	PWM	PWM 8 bit bias DAC, 4 - 16 bits signal DAC
Package	TQFP44, die		SO28, TQFP32, die		TQFP64, die
Availability	yes	samples Q2/01	yes	samples Q2/01	yes

Table 1.3: List of the XE8000 family members functions

Contacting XEMICS

You can contact XEMICS at
XEMICS SA
Tel: +41 32 720 5170
Fax: +41 32 720 5770
E-mail: info@xemics.ch

You will find more information about the XE88LC03 and other XEMICS products, as well as addresses of our representatives and distributors for your region on www.xemics.ch.

Low-Power Microcontroller
XX-XE88LC01