



**QPP-007**  
**35W, 869-894MHz**  
**Class AB Driver Stage**

**QuikPAC Module Data**

**General description:**

The **QPP-007 QuikPAC™** RF power module is an impedance matched Class AB amplifier stage designed for use in the driver stage of linear RF power amplifiers for cellular base stations. The power transistor is fabricated using Xemod's advanced design LDMOS process. The gate terminal is connected directly to the control voltage pin, allowing direct control of the bias. The user must supply the proper value of  $V_{GS}$  to set the desired quiescent current.

**Features:**

Single Polarity Operation  
 Matched for 50  $\Omega$  RF interfaces  
 XeMOS FET Technology  
 Stable Performance  
 QuikPAC System Compatible  
 QuikClip or Flange Mounting

**Standard Operating Conditions**

Parameter	Symbol	Min	Nom	Max	Units
Frequency Range	F	869		894	MHz
Supply (Drain) Voltage	$V_D$	26.0	28.0	32.0	VDC
Bias (Gate) Voltage	$V_G$	3.0	3.5	5.0	VDC
Bias (Gate) Current, Average	$I_G$			1.0	mA
RF Source & Load Impedance	$\Omega$		50		Ohms
Load Impedance for Stable Operation (All Phases)	VSWR			10:1	
Operating Baseplate Temperature	$T_{OP}$	-20		+90	$^{\circ}C$
Output Device Thermal Resistance, Channel to Baseplate	$\Theta_{jc}$		1.9		$^{\circ}C/W$

**Maximum Ratings**

Parameter	Symbol	Value	Units
Supply (Drain) Voltage	$V_{DD}$	35	VDC
Control (Gate) Voltage, $V_{DD} = 0$ VDC	$V_G$	15	VDC
Input RF Power	$P_{IN}$	2.5	W
Load Impedance for continuous operation without damage	VSWR	3:1	
Output Device Channel Temperature		200	$^{\circ}C$
Lead Soldering Temperature		+190	$^{\circ}C$
Storage Temperature	$T_{STG}$	-65 to +150	$^{\circ}C$

**Performance at 28VDC & 25 $^{\circ}C$**

Parameter	Symbol	Min	Nom	Max	Units
Supply (Drain) Voltage	$V_{D1,2}$	27.5	28.0	28.5	VDC
Quiescent Current (total) (1)	$I_{DQ}$	270	300	330	mA
Power Output at 1 dB Compression (single tone)	$P_{-1}$	35	40		W
Gain at 7W PEP (two tone)	G	14.5	15.5		dB
Gain Variation over frequency at 7W Output (two tone)	$\Delta G$		0.2	0.5	dB
Input Return Loss (50 $\Omega$ Ref) at 7W PEP (two tone)	IRL	12.0	15.0		dB
Drain Efficiency at 35W $P_{out}$ (single tone)	$\eta$	40	45		%
Drain Efficiency at 35W PEP (two tone)	$\eta$	33	36		%
3 <sup>rd</sup> Order IMD Product (2 tone at 35W PEP; 1 MHz spacing)			-30	-27	dBc

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## Performance at 28VDC & 25°C (continued)

Parameter	Symbol	Min	Nom	Max	Units
IMD Variation – 100 kHz to 25 MHz tone spacing			1.0	2.0	dB
2 <sup>nd</sup> Harmonic at 35W P <sub>out</sub> (single tone)			-40		dBc
3 <sup>rd</sup> Harmonic at 35W P <sub>out</sub> (single tone)			-45		dBc
Group (Signal) Delay	$\tau_d$		3.5		ns
Transmission Phase Flatness			0.5		degrees
CDMA ACPR at 7W P <sub>avg</sub>			-46		dB
CDMA ACPR at 3.5W P <sub>avg</sub>			-49		dB
Drain Efficiency at 7W CDMA	$\eta$	20	22		%
Drain Efficiency at 3.5W CDMA	$\eta$	14	15		%

### Notes:

This QuikPAC module requires an externally supplied gate voltage ( $V_{GS}$ ) on the gate lead (pin 3) to set the operating point (quiescent current-  $I_{DQ}$ ) of the power transistor.  $V_{GS}$  may be safely set to any voltage in the range listed in the table. This permits a wide range of quiescent current to be used. Since the operating characteristics of the module will vary as  $I_{DQ}$  changes, the bias setting will depend on the application. The data provided in the Performance section of this data sheet was obtained with  $I_{DQ}$  set to a value within the range listed (a nominal value  $\pm 10\%$ ). This particular value was chosen to optimize gain, IMD performance, and efficiency simultaneously.

Gate voltage must be applied coincident with or after application of the drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is terminated on both input and output.

The  $V_{GS}$  corresponding to a specific  $I_{DQ}$  will vary from module to module. This is due to the normal die-to-die variation in threshold voltage of LDMOS transistors.

Since the gate bias of an LDMOS transistor changes with device temperature, it may be necessary to use a  $V_{GS}$  supply with thermal compensation if operation over a wide temperature range is required.

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

The RF leads are internally protected against DC voltages up to 100V. Care should be taken to avoid video transients that may damage the active devices.

### Package Styles

This model is available in both A (H10535) and AF (H10890) package styles. Style AF is shown for reference. Please see the applicable outline drawing for specific dimensions.

