



**QPP-022**  
**180W, 869-894MHz**  
**Class AB Power Stage**

**QuikPAC Module Data**

**General description:**

The **QPP-022 QuikPAC™** RF power module is an impedance matched Class AB amplifier stage designed for use in the output stage of linear RF power amplifiers for cellular base stations. The power transistors are fabricated using Xemod's advanced design LDMOS process. This unit has a factory set, regulated and temperature compensated gate bias, eliminating the need for the user to provide adjustable gate bias voltage circuits and make individual bias adjustments during stage alignment.

**Features:**

- Single Polarity Operation
- Matched for 50 Ω RF interfaces
- XeMOS FET Technology
- Stable Performance
- QuikPAC System Compatible
- QuikClip or Flange Mounting

**Standard Operating Conditions**

Parameter	Symbol	Min	Nom	Max	Units
Frequency Range	F	869		894	MHz
Supply (Drain) Voltage	V <sub>D</sub>	26.0	28.0	32.0	VDC
Bias (Gate) Voltage	V <sub>G</sub>	11.0	12.0	13.0	VDC
Bias (Gate) Current, Average	I <sub>G</sub>			40	mA
RF Source & Load Impedance	Ω		50		Ohms
Load Impedance for Stable Operation (All Phases)	VSWR			10:1	
Operating Baseplate Temperature	T <sub>OP</sub>	-20		+90	°C
Output Device Thermal Resistance, Channel to Baseplate	θ <sub>jc</sub>		0.4		°C/W

**Maximum Ratings**

Parameter	Symbol	Value	Units
Supply (Drain) Voltage	V <sub>D</sub>	35	VDC
Control (Gate) Voltage, V <sub>D</sub> = 0 VDC	V <sub>G</sub>	15	VDC
Input RF Power	P <sub>IN</sub>	20	W
Load Impedance for continuous operation without damage	VSWR	3:1	
Output Device Channel Temperature		200	°C
Lead Soldering Temperature		+190	°C
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C

**Performance at 28VDC & 25°C**

Parameter	Symbol	Min	Nom	Max	Units
Supply (Drain) Voltage	V <sub>D1,2</sub>	27.8	28.0	28.2	VDC
Quiescent Current (total)	I <sub>DQ</sub>	1,600	1,800	2,000	mA
Peak Envelope Power at 1 dB Compression (two tone)	P <sub>-1</sub>	180	200		W
Gain at 36W PEP (two tone)	G	13.0	13.5		dB
Gain Variation over frequency at 36W PEP (two tone)	ΔG		0.3	0.5	dB
Input Return Loss (50 Ω Ref) at 36W PEP (two tone)	IRL	12	15		dB
Drain Efficiency at 180W PEP (two tone)	η	30	33		%
3 <sup>rd</sup> Order IMD Product (2 tone at 180W PEP; 1 MHz spacing)			-30	-28	dBc

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## Performance at 28VDC & 25°C (continued)

Parameter	Symbol	Min	Nom	Max	Units
IMD Variation – 100 kHz to 25 MHz tone spacing			1.0	2.0	dB
2 <sup>nd</sup> Harmonic at 180W P <sub>out</sub> (single tone)					dBc
3 <sup>rd</sup> Harmonic at 180W P <sub>out</sub> (single tone)					dBc
Group (Signal) Delay	$\tau_d$	4.7		4.9	ns
Transmission Phase Flatness			0.5	1.0	degrees
CDMA ACPR at 36W P <sub>out</sub> AVG		46	47		dB
CDMA ACPR at 18W P <sub>out</sub> AVG		52	53		dB
CDMA Drain Efficiency at 36W P <sub>out</sub> AVG	$\eta$	18	20		%
CDMA Drain Efficiency at 18W P <sub>out</sub> AVG	$\eta$	11	13		%

## Performance at 28VDC Over Temperature

Parameter	Symbol	Min	Nom	Max	Units
Peak Envelope Power at 1 dB Compression (two-tone)	$P_{-1}$	180			W
Gain at 180W PEP (two tone)	$G$				
Gain Variation over frequency at 36W PEP (two tone)	$\Delta G$				dB
Input Return Loss (50 $\Omega$ Ref) at 36W PEP (two tone)	IRL				dB
Drain Efficiency at 180W PEP (two tone)	$\eta$				%
3 <sup>rd</sup> Order IMD Product (2 tone at 180W PEP;1 MHz spacing)					dBc
Group (Signal) Delay	$\tau_d$	4.65		4.95	ns
Transmission Phase Flatness			0.5	1.0	degrees

### Notes:

This GR-version QuikPAC module has an internally regulated gate voltage that is preset at the factory. A voltage of +12VDC ( $\pm 1V$ ) should be applied to each gate lead (pins 1 and 5). No further adjustment is required. The gate voltage is thermally compensated for operation over the temperature range listed in the data sheet. Although the module will operate with lower voltages applied, the internal regulator is not functioning and the specified performance may not be achieved.

Gate voltage must be applied coincident with or after application of the drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is terminated on both input and output.

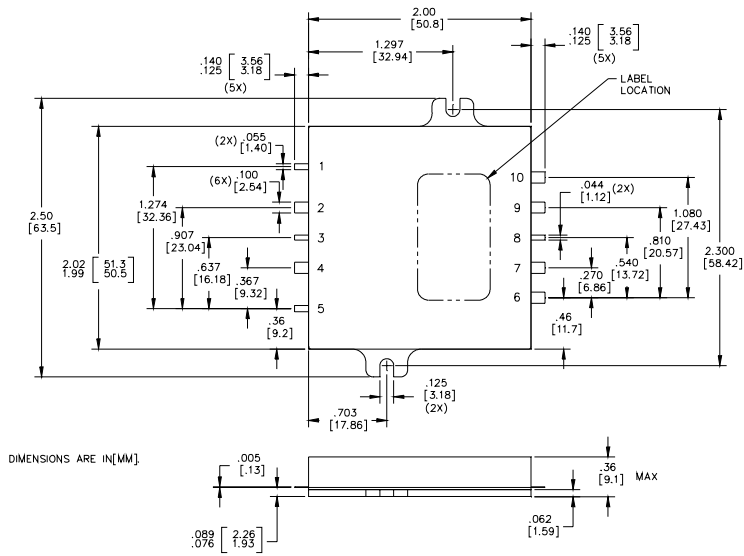
The quiescent current set during manufacture will be within the range specified in the Performance section (nominal  $\pm 10\%$ ) and is selected to balance IMD, input return loss, and efficiency. This setting is suitable for most applications. Modules with different optimization profiles are available by special order.

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

The RF leads are internally protected against DC voltages up to 100V. Care should be taken to avoid video transients that may damage the active devices.

## Package Styles

This model is available in both C (H10549) and CF (H10895) package styles. Style CF is shown for reference. Please see the applicable outline drawing for specific dimensions.



LEAD IDENTIFICATION	
Lead No.	Function
1	Bias 1
2	Ground
3	Input
4	Ground
5	Bias 2
6	Ground
7	Ground
8	Output
9	Ground
10	V <sub>DD1</sub>