Preliminary
QuikPAC Module Data

QPP-034
200W, 832-870MHz
Class AB Power Stage

General description:

The **QPP-034 QuikPAC™** RF power module is an impedance-matched Class AB amplifier stage designed for use in the output stage of linear RF power amplifiers for CDMA base stations. The power transistors are fabricated using Xemod's advanced design LDMOS process. This unit has a factory set, regulated and temperature compensated gate bias, eliminating the need for the user to provide adjustable gate bias voltage circuits and make individual bias adjustments during stage alignment.

Features:
Single Polarity Operation
Matched for 50 Ω RF interfaces
XeMOS FET Technology
Stable Performance
QuikPAC System Compatible
QuikClip or Flange Mounting

Standard Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units
Frequency Range	F	832		870	MHz
Supply (Drain) Voltage	V_D	26.0	28.0	32.0	VDC
Bias (Gate) Voltage	V_G	11.0	12.0	13.0	VDC
Bias (Gate) Current, Average	I_G			40	mA
RF Source & Load Impedance	Ω		50		Ohms
Load Impedance for Stable Operation (All Phases)	VSWR			10:1	
Operating Baseplate Temperature	T_{OP}	-20		+90	ºC
Output Device Thermal Resistance, Channel to Baseplate	Θjc		0.4		ºC/W

Maximum Ratings

Parameter	Symbol	Value	Units
Supply (Drain) Voltage	V_D	35	VDC
Control (Gate) Voltage, V_D = 0 VDC	V_G	15	VDC
Input RF Power	P_{IN}	20	W
Load Impedance for continuous operation without damage	VSWR	3:1	
Output Device Channel Temperature		200	ºC
Lead Temperature during reflow soldering		+210	ºC
Storage Temperature	T_{STG}	-65 to +150	ºC

Performance at 28VDC & 25ºC

Parameter	Symbol	Min	Nom	Max	Units
Supply (Drain) Voltage	$V_{D1,2}$	27.8	28.0	28.2	VDC
Quiescent Current (total)	I_{DQ}	1,800	2,000	2,200	mA
Peak Envelope Power at 1 dB Compression (two tone)	P_{-1}	200	220		W
Gain at 40W PEP (two tone)	G	13.0	13.5		dB
Gain Variation over frequency at 40W PEP (two tone)	ΔG		0.2	0.5	dB
Input Return Loss (50 Ω Ref) at 40W PEP (two tone)	IRL	11.0	15.0		dB
Drain Efficiency at 200W PEP (two tone)	η	32	36		%
3rd Order IMD Product (2 tone at 200W PEP;1 MHz spacing)			-30	-28	dBc
IMD Variation – 100 kHz to 25 MHz tone spacing			1.0	2.0	dB
2nd Harmonic at 200W P_{out}(single tone)					dBc
3rd Harmonic at 200W P_{out}(single tone)					dBc

Performance at 28VDC & 25ºC (continued)

Parameter	Symbol	Min	Nom	Max	Units
Group (Signal) Delay	τ_d	4.7		4.9	ns
Transmission Phase Flatness			0.5	1.0	degrees
CDMA(1) ACPR at 40W Pout AVG		-46	-48		dB
CDMA(1) ACPR at 20W Pout AVG		-52	-53		dB
CDMA(1) Drain Efficiency at 40W Pout AVG	η	20	21		%
CDMA(1) Drain Efficiency at 20W Pout AVG	η	13	15		%

Performance at 28VDC Over Temperature

Parameter	Symbol	Min	Nom	Max	Units
Peak Envelope Power at 1 dB Compression (two-tone)	P_{-1}	200			W
Gain at 200W PEP (two tone)	G				
Gain Variation over frequency at 40W Output (single tone)	ΔG				dB
Input Return Loss (50 Ω Ref) at 40W PEP (two tone)	IRL				dB
Drain Efficiency at 200W PEP (two tone)	η				%
3rd Order IMD Product (2 tone at 200W PEP;1 MHz spacing)			-29	-27	dBc
Group (Signal) Delay	τ_d	4.65		4.95	ns
Transmission Phase Flatness			0.5	1.0	degrees

(1) CDMA test signal is single carrier IS-95

Notes:

The "Preliminary" designation on this data sheet indicates this product has not yet entered the volume production stage. The data supplied here is derived from engineering development and pilot production testing and may change.

This GR-version QuikPAC module has an internally regulated gate voltage that is preset at the factory. A voltage of +12VDC (±1V) should be applied to each gate lead (pins 1 and 5). No further adjustment is required. Although the module will operate with lower voltages applied, the internal regulator is not functioning and the specified performance may not be achieved.

The internal gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be provided with AGC external to the module

Gate voltage must be applied coincident with or after application of the drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is terminated on both input and output.

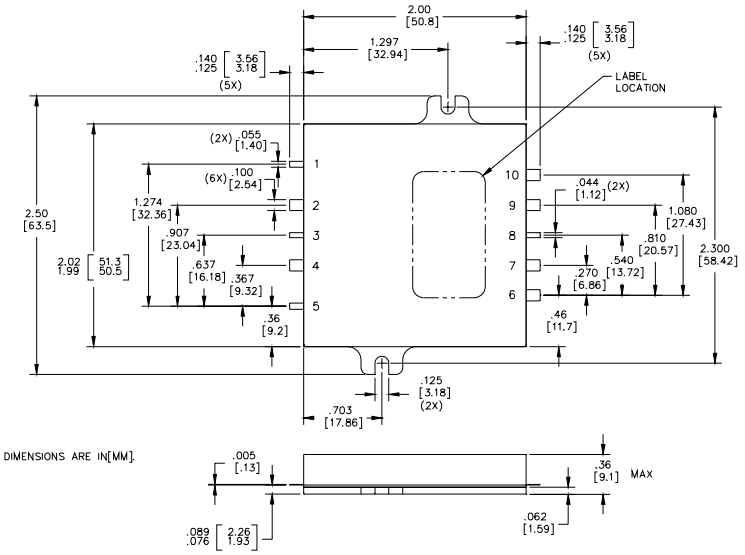
The quiescent current set during manufacture will be within the range specified in the Performance section (nominal ±10%) and is selected to balance IMD, input return loss, and efficiency. This setting is suitable for most applications. Modules with different optimization profiles are available by special order.

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

The RF leads are internally protected against DC voltages up to 100V. Care should be taken to avoid video transients that may damage the active devices.

Package Styles

This model is available in both C1 (H10549) and C1F (H10895) package styles. Style C1F is shown for reference. Please see the applicable outline drawing for specific dimensions.



LEAD IDENTIFICATION	
Lead No.	Function
1	Bias 1
2	Ground
3	Input
4	Ground
5	Bias 2
6	V_{DD2}
7	Ground
8	Output
9	Ground
10	V_{DD1}