Preliminary
QuikPAC Module Data

QPP-035
200W, 851-866MHz
Class AB Power Stage

General description:

The **QPP-035 QuikPAC™** RF power module is an impedance matched Class AB amplifier stage designed for use in the output stage of linear RF power amplifiers for SMR base stations. The power transistors are fabricated using Xemod's advanced design LDMOS process. The gate terminal is connected directly to the control voltage pin, allowing direct control of the bias. The user must supply the proper value of V_{GS} to set the desired quiescent current.

Features:
Single Polarity Operation
Matched for 50 Ω RF interfaces
XeMOS FET Technology
Stable Performance
QuikPAC System Compatible
QuikClip or Flange Mounting

Standard Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units
Frequency Range	F	851		866	MHz
Supply (Drain) Voltage	V_D	26.0	28.0	32.0	VDC
Bias (Gate) Voltage	V_G	3.0	3.5	5.0	VDC
Bias (Gate) Current, Average	I_G			2.0	mA
RF Source & Load Impedance	Ω		50		Ohms
Load Impedance for Stable Operation (All Phases)	VSWR			10:1	
Operating Baseplate Temperature	T_{OP}	-20		+90	ºC
Output Device Thermal Resistance, Channel to Baseplate	Θjc		0.4		ºC/W

Maximum Ratings

Parameter	Symbol	Value	Units
Supply (Drain) Voltage	V_D	35	VDC
Control (Gate) Voltage, V_D = 0 VDC	V_G	15	VDC
Input RF Power	P_{IN}	20	W
Load Impedance for continuous operation without damage	VSWR	3:1	
Output Device Channel Temperature		200	ºC
Lead Temperature during reflow soldering		+210	ºC
Storage Temperature	T_{STG}	-65 to +150	ºC

Performance at 28VDC & 25ºC

Parameter	Symbol	Min	Nom	Max	Units
Supply (Drain) Voltage	$V_{D1,2}$	27.8	28.0	28.2	VDC
Quiescent Current (total)	I_{DQ}	1,800	2,000	2,200	mA
Peak Envelope Power at 1 dB Compression (two tone)	P_{-1}	200	220		W
Gain at 40W PEP (two tone)	G	13.5	14.0		dB
Gain Variation over frequency at 40W Output (two tone)	ΔG		0.2	0.5	dB
Input Return Loss (50 Ω Ref) at 40W PEP (two tone)	IRL	12.0	15.0		dB
Drain Efficiency at 200W PEP (two tone)	η	32	36		%
3rd Order IMD Product (2 tone at 200W PEP;1 MHz spacing)			-30	-28	dBc
IMD Variation – 100 kHz to 25 MHz tone spacing			1.0	2.0	dB
2nd Harmonic at 200W P_{out}(single tone)					dBc
3rd Harmonic at 200W P_{out}(single tone)					dBc

Performance at 28VDC & 25ºC (continued)

Parameter	Symbol	Min	Nom	Max	Units
Group (Signal) Delay	τ_d	4.7		4.9	ns
Transmission Phase Flatness			0.5	1.0	degrees

Notes:

The "Preliminary" designation on this data sheet indicates this product has not yet entered the volume production stage. The data supplied here is derived from engineering development and pilot production testing and may change.

This QuikPAC module requires an externally supplied gate voltage (V_{GS}) on each gate lead (pins 1 and 5) to set the operating point (quiescent current (I_{DQ})) of the power transistors. V_{GS} may be safely set to any voltage in the range listed in the table. This permits a wide range of quiescent current to be used. Since the operating characteristics of the module will vary as I_{DQ} changes, the proper bias setting will depend on the application. The data provided in the Performance section of this data sheet was obtained with I_{DQ} set to a value within the range listed (a nominal value ±10%). This particular value was chosen to provide a gain, IMD performance, and efficiency that are suitable for many applications but may not be optimum for a specific design requirement.

Gate voltage must be applied coincident with or after application of the drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is terminated on both input and output.

The V_{GS} corresponding to a specific I_{DQ} will vary from module to module and may vary between the two sides of a dual RF module by as much as ±0.10 volts. This is due to the normal die-to-die variation in threshold voltage of LDMOS transistors.

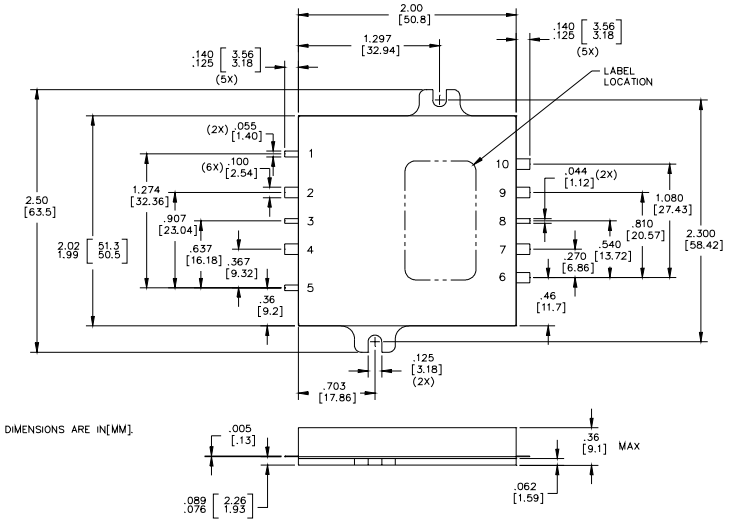
Since the threshold voltage of an LDMOS transistor changes with temperature, it is usually necessary to use a V_{GS} supply that is compensated to maintain constant I_{DQ} over temperature if operation over a wide temperature range is desired.

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

The RF leads are internally protected against DC voltages up to 100V. Care should be taken to avoid video transients that may damage the active devices.

Package Styles

This model is available in both C1 (H10549) and C1F (H10895) package styles. Style C1F is shown for reference. Please see the applicable outline drawing for specific dimensions.



LEAD IDENTIFICATION	
Lead No.	Function
1	Bias 1
2	Ground
3	Input
4	Ground
5	Bias 2
6	V_{DD2}
7	Ground
8	Output
9	Ground
10	V_{DD1}