**Preliminary**
**QuikPAC Module Data**

# QPP-307
# 60W; 2110-2170MHz
# Class AB Power Stage

## General description:

The **QPP-307 QuikPAC™** RF power module is an impedance matched Class AB amplifier stage designed for use in the driver or output stage of linear RF power amplifiers for cellular base stations. The power transistors are fabricated using Xemod's advanced design LDMOS process. The gate terminal is connected directly to the control voltage pin, allowing direct control of the bias. The user must supply the proper value of $V_{GS}$ to set the desired quiescent current.

**Features:**
Single Polarity Operation
Matched for 50 Ω RF interfaces
XeMOS FET Technology
Stable Performance
QuikPAC System Compatible
QuikClip or Flange Mounting

## Standard Operating Conditions

| Parameter | Symbol | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Frequency Range | F | 2110 | | 2170 | MHz |
| Supply (Drain) Voltage | $V_D$ | 26.0 | 28.0 | 32.0 | VDC |
| Bias (Gate) Voltage | $V_G$ | 3.0 | 3.5 | 5.0 | VDC |
| Bias (Gate) Current, Average | $I_G$ | | | 2.0 | mA |
| RF Source & Load Impedance | Ω | | 50 | | Ohms |
| Load Impedance for Stable Operation (All Phases) | VSWR | | | 10:1 | |
| Operating Baseplate Temperature | $T_{OP}$ | -20 | | +90 | ºC |
| Output Device Thermal Resistance, Channel to Baseplate | Θjc | | 1.1 | | ºC/W |

## Maximum Ratings

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Supply (Drain) Voltage | $V_D$ | 35 | VDC |
| Control (Gate) Voltage, $V_D$ = 0 VDC | $V_G$ | 15 | VDC |
| Input RF Power | $P_{IN}$ | 5 | W |
| Load Impedance for continuous operation without damage | VSWR | 3:1 | |
| Output Device Channel Temperature | | 200 | ºC |
| Lead Soldering Temperature | | +190 | ºC |
| Storage Temperature | $T_{STG}$ | -65 to +150 | ºC |

## Performance at 28VDC & 25ºC

| Parameter | Symbol | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Supply (Drain) Voltage | $V_{D1}$ | 27.8 | 28.0 | 28.2 | VDC |
| Quiescent Current (total) | $I_{DQ}$ | 540 | 600 | 660 | mA |
| Power Output at 1 dB Compression (single tone) | $P_{-1}$ | 60 | | | W |
| Gain at 12W PEP (two tone) | G | 11.0 | 12.0 | | dB |
| Gain Variation over frequency at 12W PEP (two tone) | ΔG | | 0.25 | 0.4 | dB |
| Input Return Loss (50 Ω Ref) at 12W PEP (two tone) | IRL | 12.0 | 14.0 | | dB |
| Drain Efficiency at 60W PEP (two tone) | η | 28 | 31 | | % |
| 3rd Order IMD Product (2 tone at 60W PEP;1 MHz spacing) | | | -30 | -28 | dBc |

## Performance at 28VDC & 25ºC (continued)

| Parameter | Symbol | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| IMD Variation – 100 kHz to 25 MHz tone spacing | | | 1.0 | 2.0 | dB |
| $2^{nd}$ Harmonic at 60W $P_{out}$(single tone) | | | | | dBc |
| $3^{rd}$ Harmonic at 60W $P_{out}$(single tone) | | | | | dBc |
| Group (Signal) Delay | $\tau_d$ | | 1.8 | | ns |
| Transmission Phase Flatness | | | 0.6 | 1.0 | degrees |
| Drain Efficiency at 12.5W W-CDMA Output | $\eta$ | 20 | 22 | | % |
| W-CDMA ACPR at 4.8W Pout (single channel) (1) | | | -46 | | dBc |
| W-CDMA ACPR at 7.6W Pout (single channel) (1) | | | -44 | | dBc |
| W-CDMA ACPR at 12.0W Pout (single channel) (1) | | | -39 | | dBc |
| W-CDMA ACPR at 2.4W Pout (2 channels at 10MHz) (1) | | | -45 | | dBc |
| W-CDMA ACPR at 3.8W Pout (2 channels at 10MHz) (1) | | | -44 | | dBc |
| W-CDMA ACPR at 6.0W Pout (2 channels at 10MHz) (1) | | | -42 | | dBc |
| W-CDMA Alt 1 at 2.4W Pout (2 channels at 10MHz) (1) | | | -43 | | dBc |
| W-CDMA Alt 1 at 3.8W Pout (2 channels at 10MHz) (1) | | | -39 | | dBc |
| W-CDMA Alt 1 at 6.0W Pout (2 channels at 10MHz) (1) | | | -37 | | dBc |

**Notes:**
(1) W-CDMA test waveform used is 3GPP Test Model 1, 64DHCP, 10.5dB Peak to Average ratio.

This QuikPAC module requires an externally supplied gate voltage ($V_{GS}$) on the gate leads (pins 1 and 5) to set the operating point (quiescent current- $I_{DQ}$) of the power transistors. $V_{GS}$ may be safely set to any voltage in the range listed in the table. The data provided in the Performance section of this data sheet was obtained with $I_{DQ}$ set to a value within the range shown (a nominal value ±10%). Since the operating characteristics of the module will vary as $I_{DQ}$ changes, the bias to be used will depend on the application.

Gate voltage must be applied coincident with or after application of the drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module without RF terminations on input and output.

The $V_{GS}$ corresponding to a specific $I_{DQ}$ will vary from module to module.. This is due to the normal die-to-die variation in threshold voltage of LDMOS transistors.

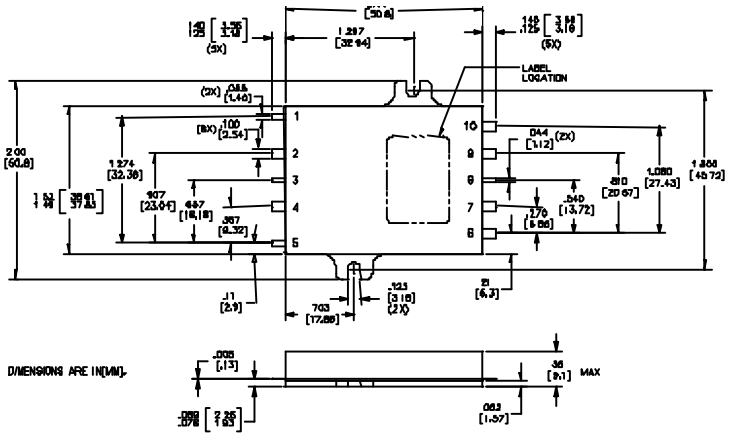
Since the gate bias of an LDMOS transistor changes with device temperature, it may be necessary to use a $V_{GS}$ supply with thermal compensation if operation over a wide temperature range is required.

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

The RF leads are internally protected against DC voltages up to 100V. Care should be taken to avoid video transients that may damage the active devices.

**Package Styles**

This model is available in both B3 (H11860) and B3F (H11861) package styles. Style B3F is shown for reference. Please see the applicable outline drawing for specific dimensions.




| LEAD IDENTIFICATION | |
|---|---|
| Lead No. | Function |
| 1 | Bias 1 |
| 2 | Ground |
| 3 | Input |
| 4 | Ground |
| 5 | N/C |
| 6 | N/C |
| 7 | Ground |
| 8 | Output |
| 9 | Ground |
| 10 | $V_{CC}$ |