Preliminary
QuikPAC Module Data

QPP-308
60W, 2110-2170MHz
Class AB Power Stage

General description:

The **QPP-308 QuikPAC™** RF power module is a Class AB amplifier stage designed for use in the driver and output stages of linear RF power amplifiers for cellular base stations. The power transistors are fabricated using Xemod's advanced design LDMOS process. This unit has a factory set, regulated and temperature compensated gate bias, eliminating the need for the user to provide adjustable gate bias voltage circuits and make individual bias adjustments during stage alignment.

Features:
Single Polarity Operation
Matched for 50 Ω RF interfaces
XeMOS FET Technology
Stable Performance
QuikPAC System Compatible
QuikClip or Flange Mounting

Standard Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units
Frequency Range	F	2110		2170	MHz
Supply (Drain) Voltage	V_D	26.0	28.0	32.0	VDC
Bias (Gate) Voltage	V_G	11.0	12.0	13.0	VDC
Bias (Gate) Current, Average	I_G			40	mA
RF Source & Load Impedance	Ω		50		Ohms
Load Impedance for Stable Operation (All Phases)	VSWR			10:1	
Operating Baseplate Temperature	T_{OP}	-20		+90	ºC
Output Device Thermal Resistance, Channel to Baseplate	Θjc				ºC/W

Maximum Ratings

Parameter	Symbol	Value	Units
Supply (Drain) Voltage	V_D	35	VDC
Control (Gate) Voltage, V_D = 0 VDC	V_G	15	VDC
Input RF Power	P_{IN}		W
Load Impedance for continuous operation without damage	VSWR	3:1	
Output Device Channel Temperature		200	ºC
Lead Soldering Temperature		+190	ºC
Storage Temperature	T_{STG}	-65 to +150	ºC

Performance at 28VDC & 25ºC

Parameter	Symbol	Min	Nom	Max	Units
Supply (Drain) Voltage	V_{D1}	27.8	28.0	28.2	VDC
Quiescent Current (total)	I_{DQ}	540	600	660	mA
Power Output at 1 dB Compression (single tone)	P_{-1}	60			W
Gain at 12W PEP (two tone)	G	11.0	12.0		dB
Gain Variation over frequency at 12W PEP (two tone)	ΔG		0.25	0.4	dB
Input Return Loss (50 Ω Ref) at 12W PEP (two tone)	IRL	12.0	14.0		dB
Drain Efficiency at 60W PEP (two tone)	η	28	31		%
3rd Order IMD Product (2 tone at 60W PEP;1 MHz spacing)			-30	-28	dBc

Performance at 28VDC & 25ºC (continued)

Parameter	Symbol	Min	Nom	Max	Units
IMD Variation – 100 kHz to 25 MHz tone spacing			1.0	2.0	dB
2nd Harmonic at 60W P_{out}(single tone)					dBc
3rd Harmonic at 60W P_{out}(single tone)					dBc
Group (Signal) Delay	τ_d		1.8		ns
Transmission Phase Flatness			0.6	1.0	degrees
Drain Efficiency at 12.5W W-CDMA Output	η	20	22		%
W-CDMA ACPR at 4.8W Pout (single channel) (1)			-46		dBc
W-CDMA ACPR at 7.6W Pout (single channel) (1)			-44		dBc
W-CDMA ACPR at 12.0W Pout (single channel) (1)			-39		dBc
W-CDMA ACPR at 2.4W Pout (2 channels at 10MHz) (1)			-45		dBc
W-CDMA ACPR at 3.8W Pout (2 channels at 10MHz) (1)			-44		dBc
W-CDMA ACPR at 6.0W Pout (2 channels at 10MHz) (1)			-42		dBc
W-CDMA Alt 1 at 2.4W Pout (2 channels at 10MHz) (1)			-43		dBc
W-CDMA Alt 1 at 3.8W Pout (2 channels at 10MHz) (1)			-39		dBc
W-CDMA Alt 1 at 6.0W Pout (2 channels at 10MHz) (1)			-37		dBc

Performance at 28VDC Over Temperature

Parameter	Symbol	Min	Nom	Max	Units
Power Output at 1 dB Compression (single tone)	P_{-1}				W
Gain Variation over frequency at 12W Output (two tone)	ΔG				dB
Input Return Loss (50 Ω Ref) at 12W Output (two tone)	IRL				dB
Drain Efficiency at 60W PEP (two tone)	η				%
3rd Order IMD Product (2 tone at 60W PEP;1 MHz spacing)			-29	-27	dBc
Group (Signal) Delay	τ_d		1.8		ns
Transmission Phase Flatness			0.6	1.0	degrees

Notes:
(1) W-CDMA test waveform used is 3GPP Test Model 1, 64DHCP, 10.5dB Peak to Average ratio.

This GR-version QuikPAC module has an internally regulated gate voltage that is preset at the factory. A voltage of +12VDC (±1V) should be applied to the gate lead (pin 1). No further adjustment is required. The gate voltage is thermally compensated for operation over the temperature range listed in the data sheet. Although the module will operate with lower voltages applied, the internal regulator is not functioning and the specified performance may not be achieved.

Gate voltage must be applied coincident with or after application of the drain voltage to prevent potentially destructive oscillations. Bias voltages should never be applied to a module unless it is terminated on both input and output.

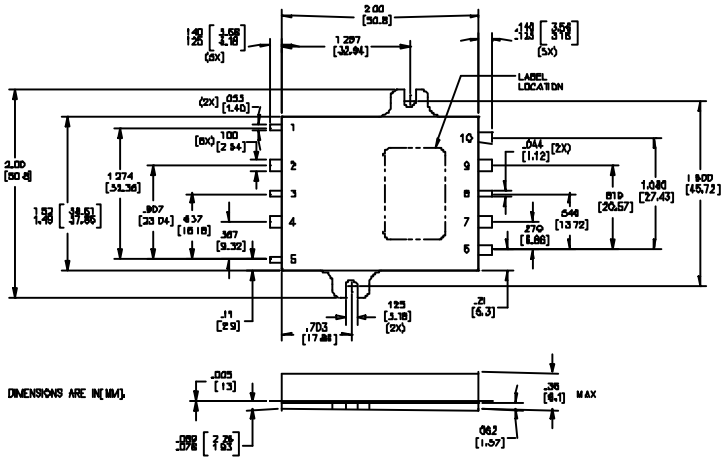
The quiescent current set during manufacture will be within the range specified in the Performance section (nominal ±10%) and is selected to balance IMD, input return loss, and efficiency. This setting is suitable for most applications. Modules with different optimization profiles are available by special order.

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

The RF leads are internally protected against DC voltages up to 100V. Care should be taken to avoid video transients that may damage the active devices.

Package Styles

This model is available in both B3 (H11860) and B3F (H11861) package styles. Style B3F is shown for reference. Please see the applicable outline drawing for specific dimensions.



LEAD IDENTIFICATION	
Lead No.	Function
1	Base 1
2	Ground
3	Input
4	Ground
5	N/C
6	N/C
7	Ground
8	Output
9	Ground
10	V_{BB}