1K Bit X22C12 256 x 4

Nonvolatile Static RAM

FEATURES

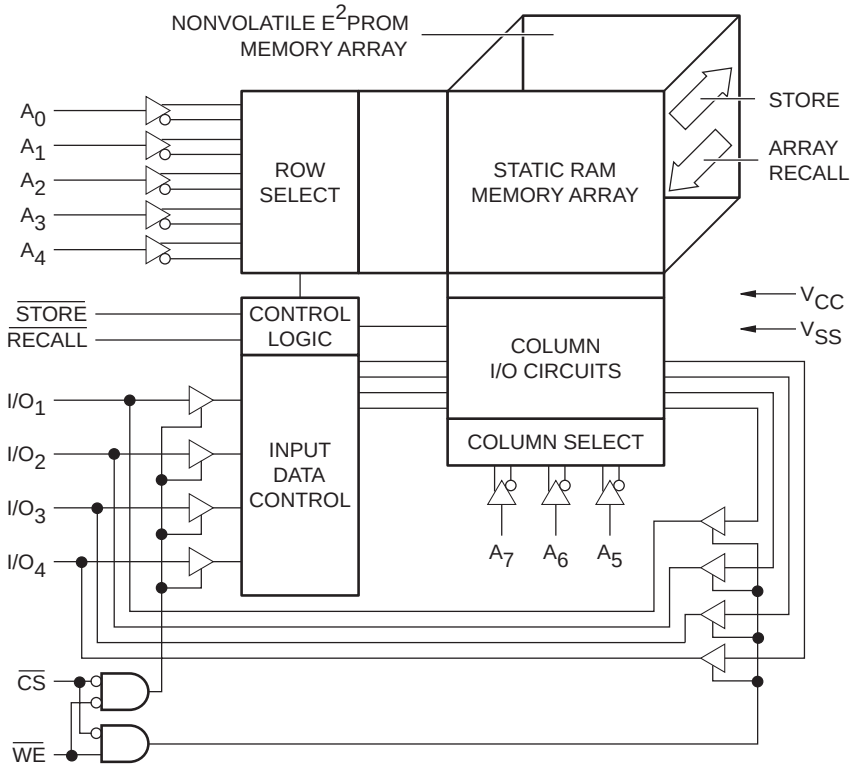
- **High Performance CMOS**
  - **—150ns RAM Access Time**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**
- **Low Power Consumption**
  - **—Active: 40mA Max.**
  - **—Standby: 100μA Max.**
- **Infinite Array Recall, RAM Read and Write Cycles**
- **Nonvolatile Store Inhibit: V_{CC} = 3.5V Typical**
- **Fully TTL and CMOS Compatible**
- **JEDEC Standard 18-Pin 300-mil DIP**
- **100% Compatible with X2212**
  - **—With Timing Enhancements**

DESCRIPTION

The X22C12 is a 256 x 4 CMOS NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E^2PROM. The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (STORE) and from E^2PROM to RAM (RECALL). The STORE operation is completed within 5ms or less and the RECALL is completed within 1μs.

Xicor NOVRAMs are designed for unlimited write operations to the RAM, either RECALLs from E^2PROM or writes from the host. The X22C12 will reliably endure 1,000,000 STORE cycles. Inherent data retention is greater than 100 years.

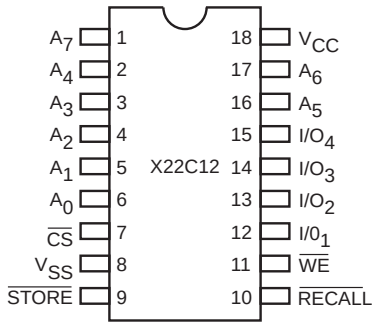
FUNCTIONAL DIAGRAM



3817 FHD F01

PIN CONFIGURATION

PLASTIC DIP
CERDIP



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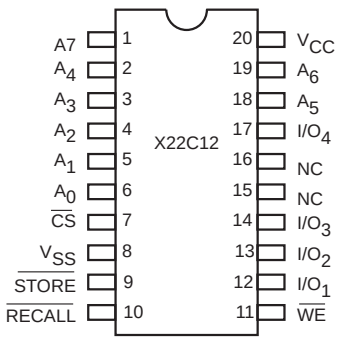

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PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_7)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read or write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. When $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH, the I/O pins will output data from the selected RAM address locations. When both $\overline{CS}$ and $\overline{WE}$ are LOW, data presented at the I/O pins will be written to the selected address location.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X22C12 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E^2PROM array. The $\overline{WE}$ and $\overline{RECALL}$ inputs are inhibited during the store cycle. The store operation is completed in 5ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E^2PROM arrays.

$\overline{RECALL}$

The $\overline{RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E^2PROM array to the RAM array. The transfer of data will be completed in 1µs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{RECALL}$ is asserted. $\overline{RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

Automatic Recall

Upon power-up the X22C12 will automatically recall data from the E^2PROM array into the RAM array.

Write Protection

The X22C12 has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V_{CC} Sense—All functions are inhibited when V_{CC} is <3.5V typical.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E^2PROM data integrity will be maintained.
- Noise Protection—A $\overline{STORE}$ pulse of typically less than 20ns will not initiate a store cycle.

PIN NAMES

Symbol	Description
A_0–A_7	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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ABSOLUTE MAXIMUM RATINGS

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X22C12	5V ±10%

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current, RAM Read/Write		40	mA	$\overline{CS}$ = V_{IL}, I/Os = Open, All Others = V_{IH}, Addresses = 0.4V/2.4V Levels @ f = 8MHz
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		2	mA	Store or Recall Functions Not Active, I/Os = Open, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		100	µA	Store or Recall functions Not Active, I/Os = Open, All Other Inputs = V_{CC} –0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	0.8	V	
V_{IH}(2)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4.2mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –2mA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

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Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	I/O	Mode
H	X	H	H	Output High Z	Not Selected(3)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write “1” RAM
L	L	H	H	Input Data Low	Write “0” RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Store(4)
H	X	H	L	Output High Z	Nonvolatile Store(4)

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ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

3817 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(5)	Power-up to Read Operation	100	µs
t_{PUW}(5)	Power-up to Write or Store Operation	5	ms

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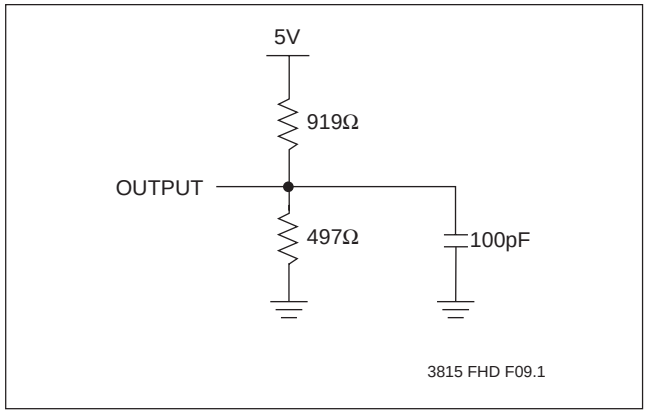
EQUIVALENT A.C. LOAD CIRCUIT



3815 FHD F09.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3817 PGM T04.1

Notes: (3) Chip is deselected but may be automatically completing a store cycle.
(4) $\overline{STORE}$ = LOW is required only to initiate the store cycle, after which the store cycle will be automatically completed (e.g. $\overline{STORE}$ = X).
(5) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	150		ns
t_{AA}	Access Time		150	ns
t_{CO}	Chip Select to Output Valid		150	ns
t_{OH}	Output Hold from Address Change	0		ns
t_{LZ}(6)	Chip Select to Output in Low Z	0		ns
t_{HZ}(6)	Chip Deselect to Output in High Z		50	ns

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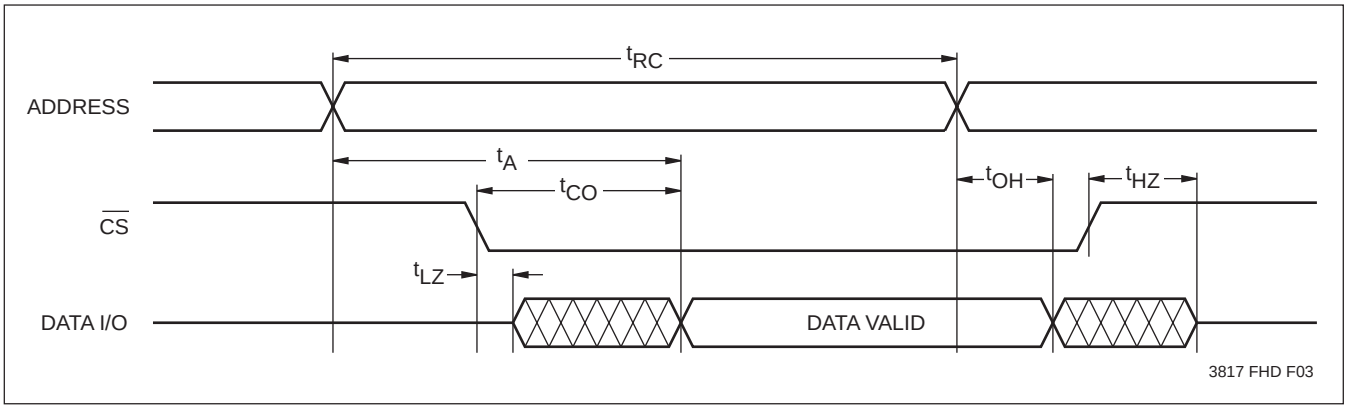
Read Cycle



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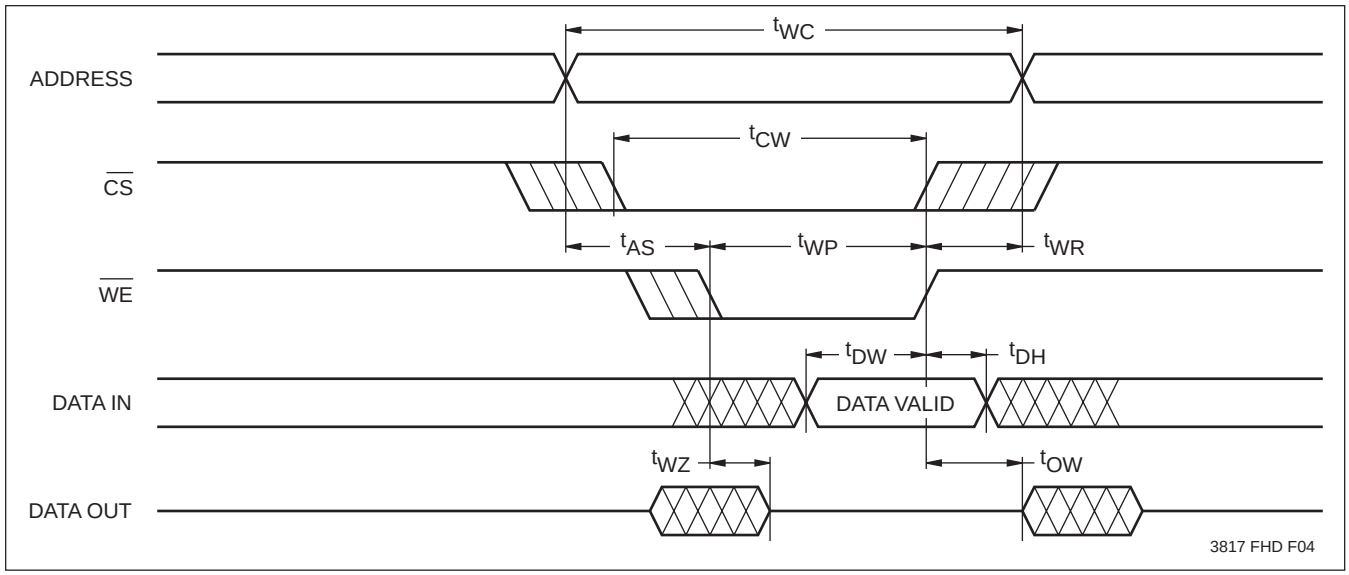
Note: (6) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

Write Cycle Limits

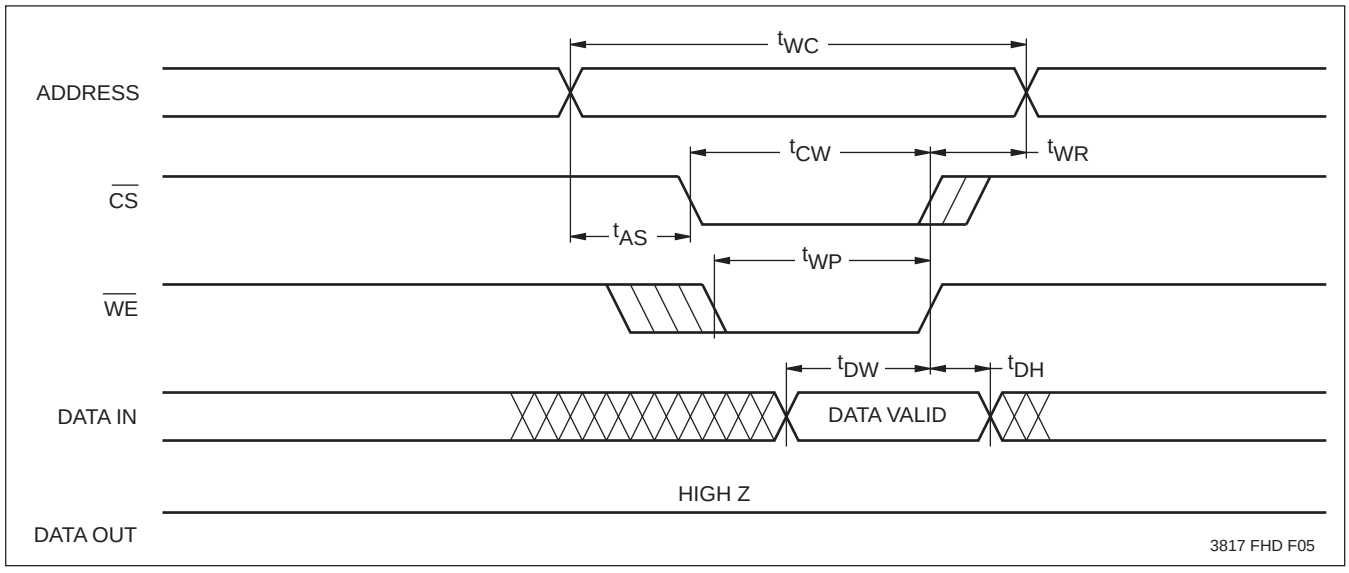
Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	150		ns
t_{CW}	Chip Select to End of Write	90		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{WR}	Write Recovery Time	0		ns
t_{DW}	Data Valid to End of Write	40		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z		50	ns
t_{OW}	Output Active from End of Write	0		ns

3817 PGM T09.1

Write Cycle



Early Write Cycle



Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Time		1	µs
t_{RCP}(7)	Recall Pulse Width	90		ns
t_{RCZ}	Recall to Output in High Z		50	ns
t_{ORC}	Output Active from End of Recall	0		ns
t_{ARC}	Recalled Data Access Time from End of Recall		120	ns

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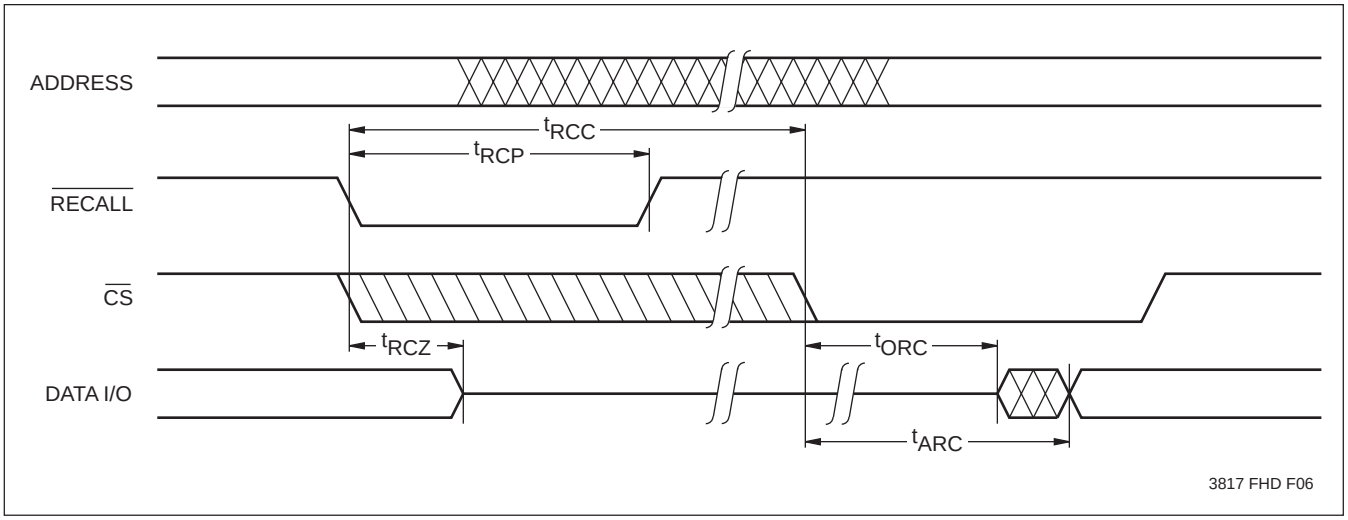
Recall Cycle



Note: (7) $\overline{\text{RECALL}}$ rise time must be less than 1µs.

Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Internal Store Time		5	ms
t_{STP}	Store Pulse Width	90		ns
t_{STZ}	Store to Output in High Z		50	ns
t_{OST}	Output Active from End of Store	0		ns

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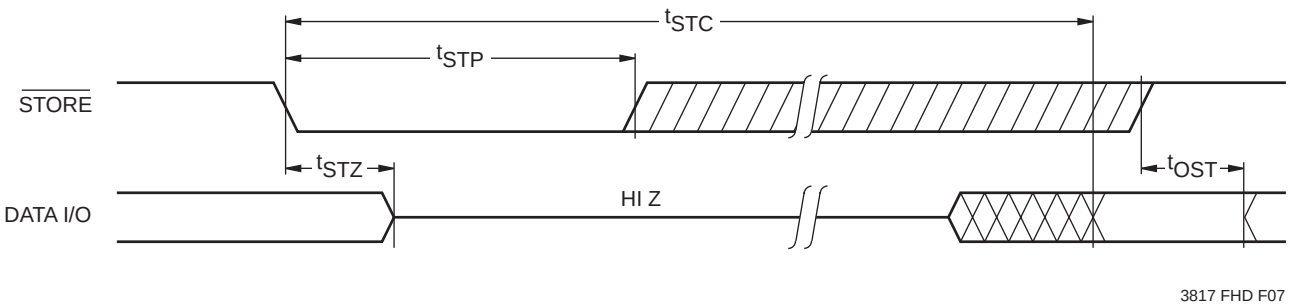
Store Cycle Limits



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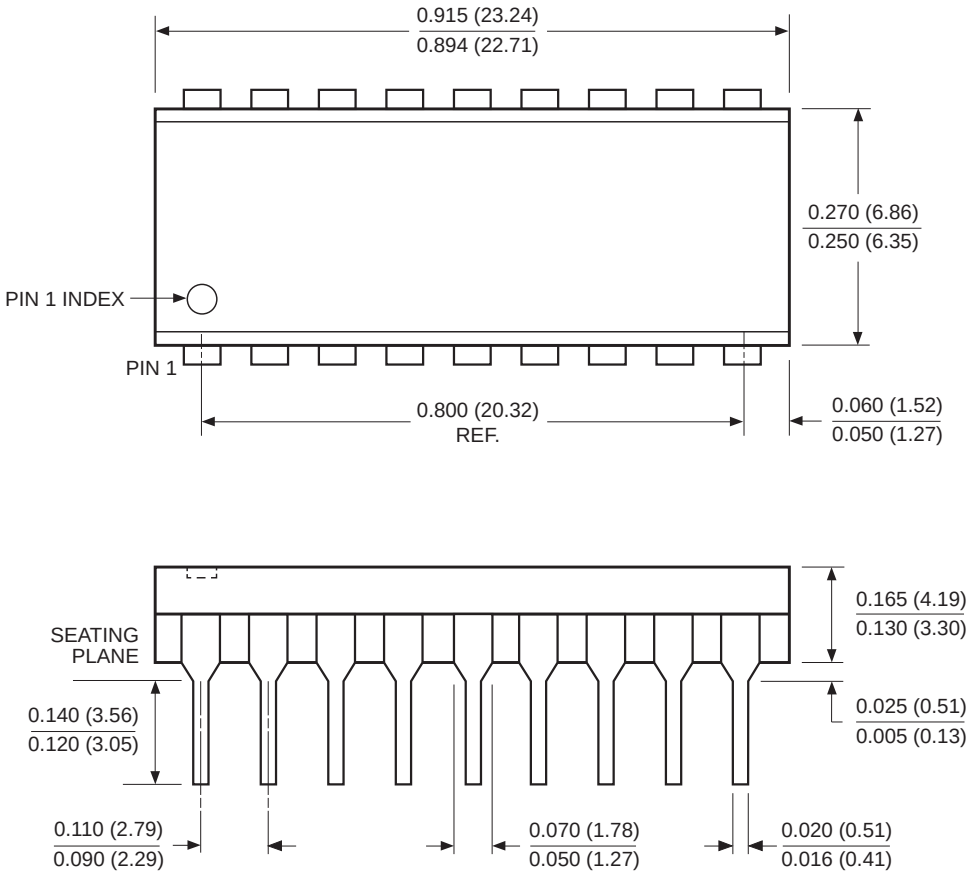
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

18-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

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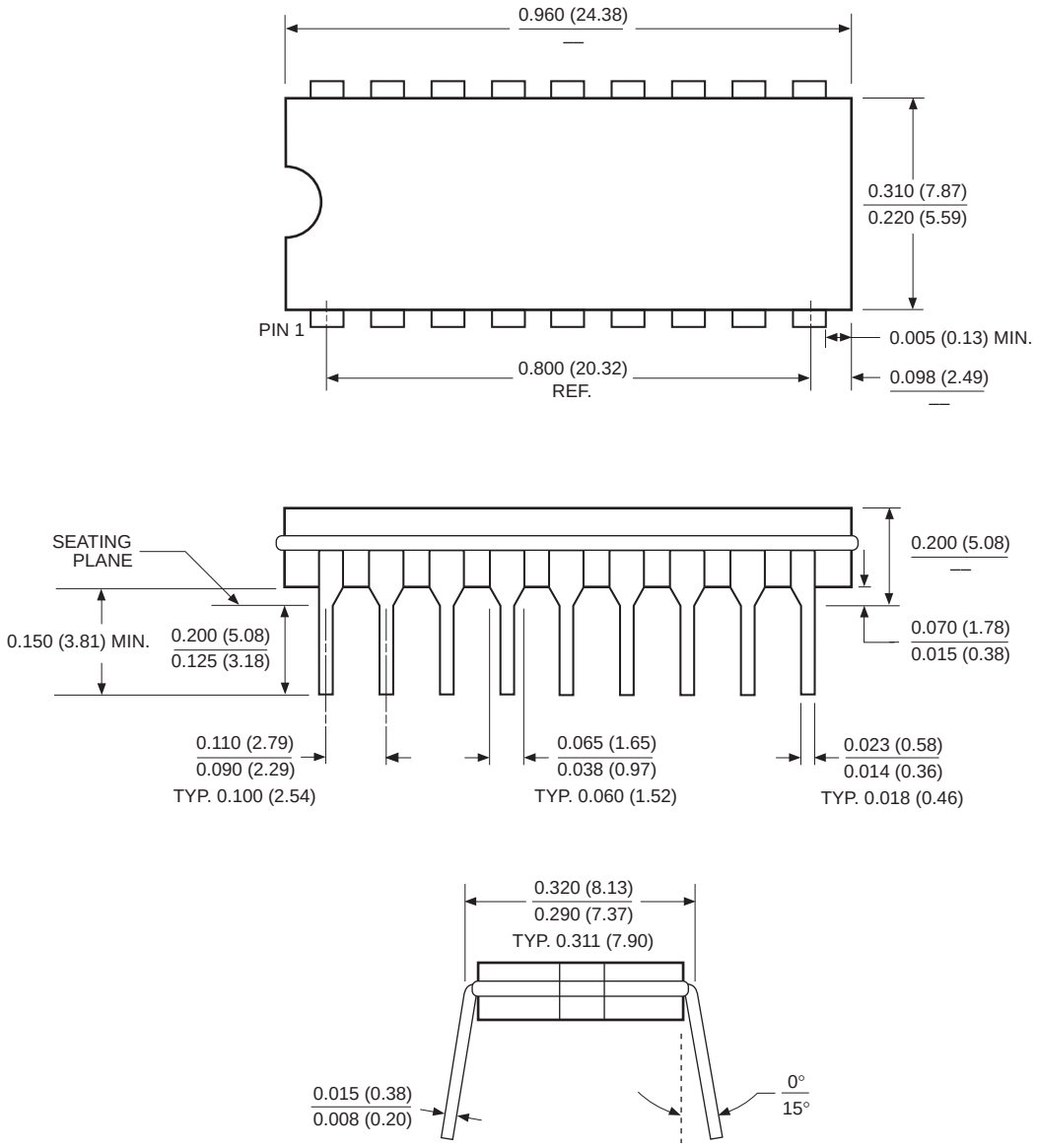
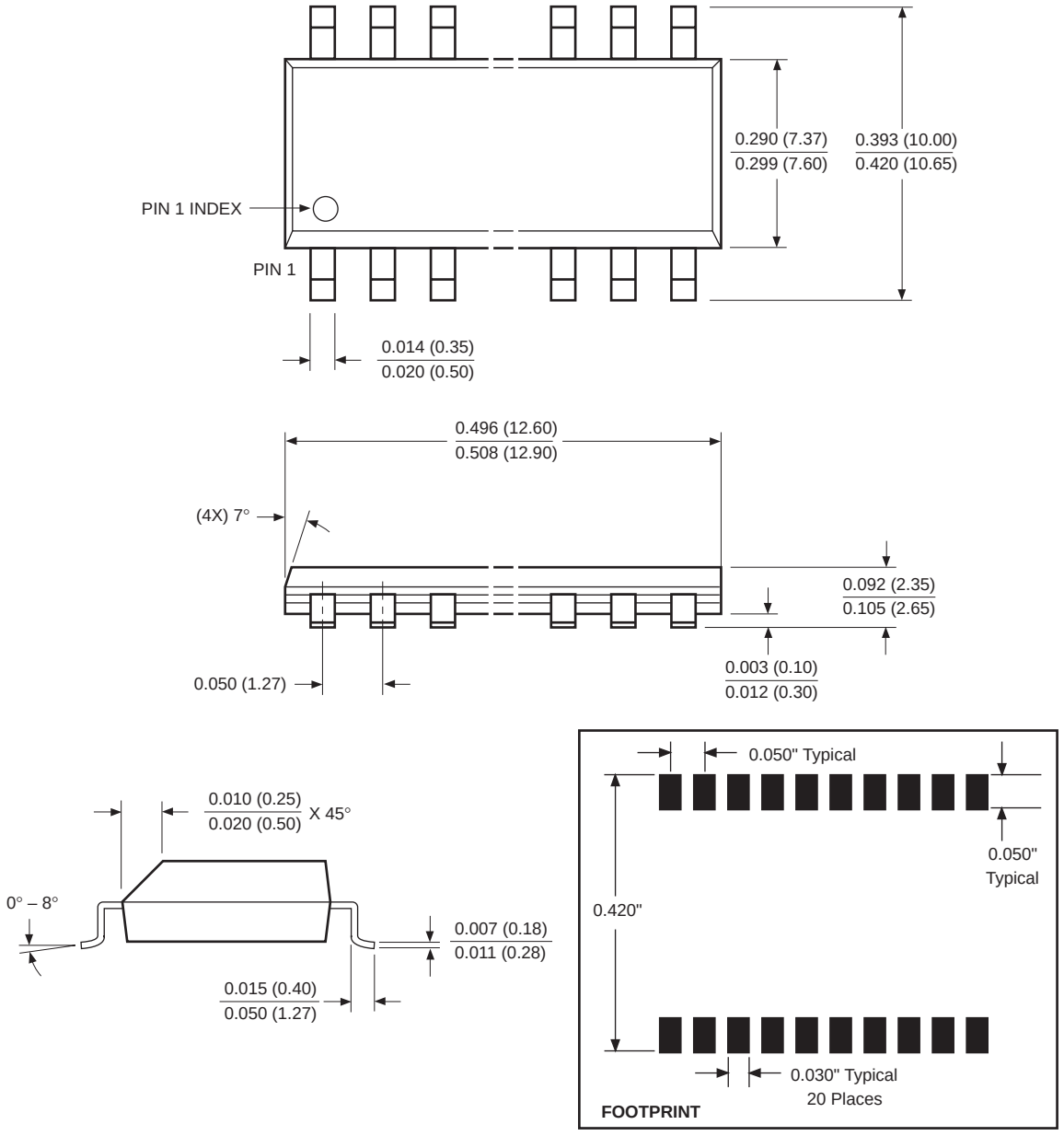
18-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F06

20-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F23

ORDERING INFORMATION