XC95144 In-System Programmable CPLD

December 4, 1998 (Version 4.0)

Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 144 macrocells with 3,200 usable gates
- Up to 133 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 100-pin PQFP, 100-pin TQFP, and 160-pin PQFP packages

Description

The XC95144 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 3,200 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95144 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95144 device.

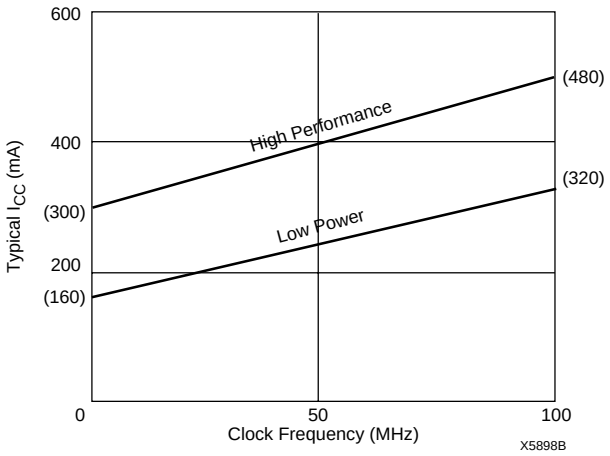


Figure 1: Typical I_{cc} vs. Frequency for XC95144

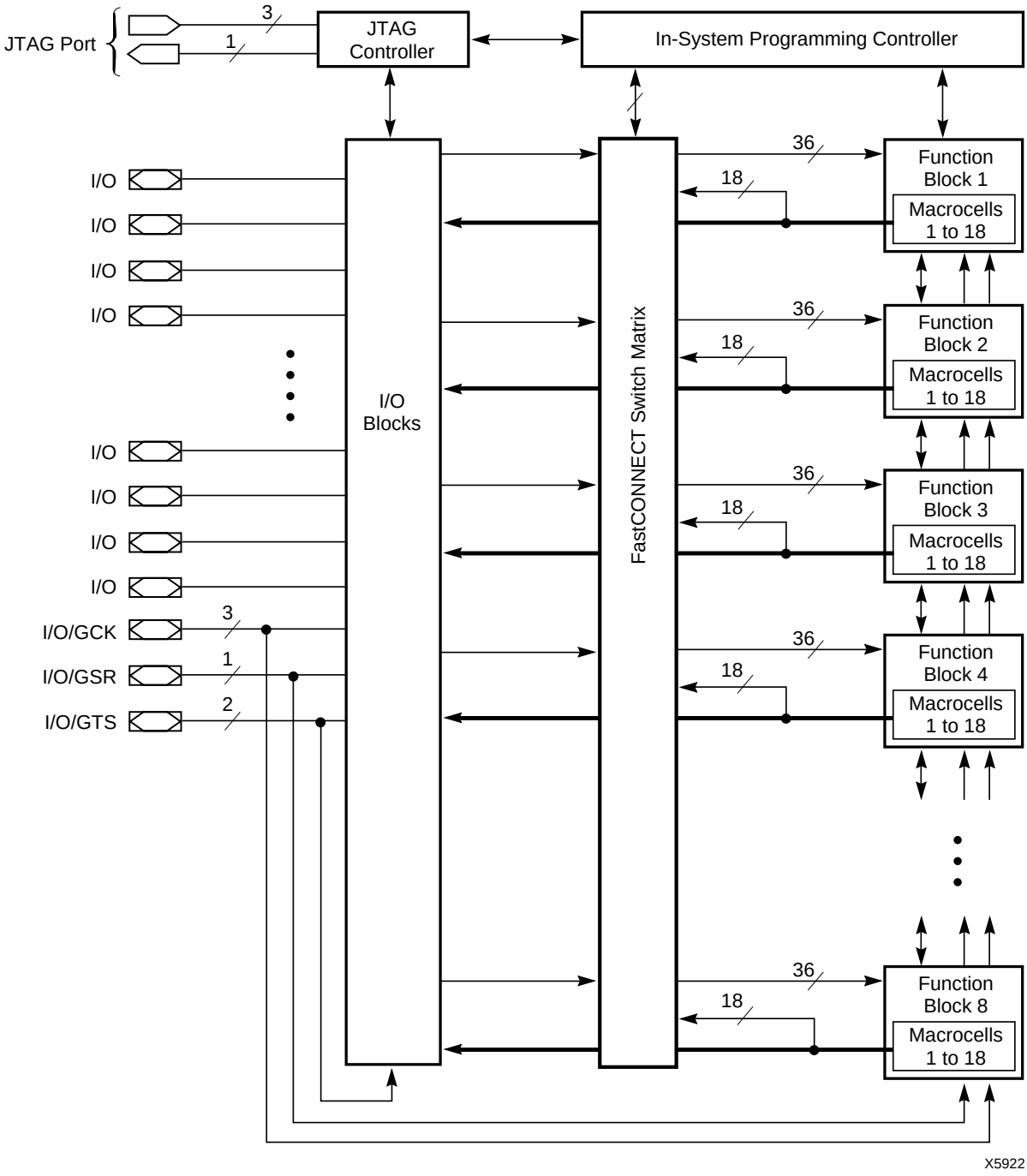


Figure 2: XC95144 Architecture

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V

Note: 1. Numbers in parenthesis are for industrial-temperature range versions.

Endurance Characteristics

Symbol	Parameter	Min	Max	Units
t_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles	10,000	-	Cycles

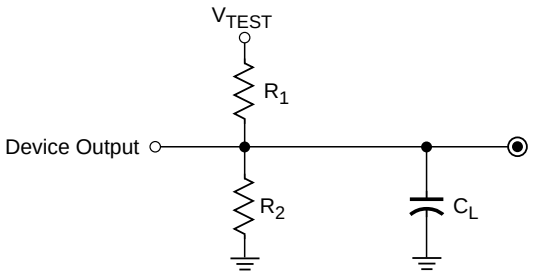
DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	160 (Typ)		ma

AC Characteristics

Symbol	Parameter	XC95144-7		XC95144-10		XC95144-15		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		7.5		10.0		15.0	ns
t_{SU}	I/O setup time before GCK	4.5		6.0		8.0		ns
t_{H}	I/O hold time after GCK	0.0		0.0		0.0		ns
t_{CO}	GCK to output valid		4.5		6.0		8.0	ns
f_{CNT} [1]	16-bit counter frequency	125.0		111.1		95.2		MHz
f_{SYSTEM} [2]	Multiple FB internal operating frequency	83.3		66.7		55.6		MHz
t_{PSU}	I/O setup time before p-term clock input	0.5		2.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	4.0		4.0		4.0		ns
t_{PCO}	P-term clock to output valid		8.5		10.0		12.0	ns
t_{OE}	GTS to output valid		5.5		6.0		11.0	ns
t_{OD}	GTS to output disable		5.5		6.0		11.0	ns
t_{POE}	Product term OE to output enabled		9.5		10.0		14.0	ns
t_{POD}	Product term OE to output disabled		9.5		10.0		14.0	ns
t_{WLH}	GCK pulse width (High or Low)	4.0		4.5		5.5		ns

Note: 1. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable.
f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
2. f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC95144-7		XC95144-10		XC95144-15		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
t_{IN}	Input buffer delay		2.5		3.5		4.5	ns
t_{GCK}	GCK buffer delay		1.5		2.5		3.0	ns
t_{GSR}	GSR buffer delay		4.5		6.0		7.5	ns
t_{GTS}	GTS buffer delay		5.5		6.0		11.0	ns
t_{OUT}	Output buffer delay		2.5		3.0		4.5	ns
t_{EN}	Output buffer enable/disable delay		0.0		0.0		0.0	ns
Product Term Control Delays								
t_{PTCK}	Product term clock delay		3.0		3.0		2.5	ns
t_{PTSR}	Product term set/reset delay		2.0		2.5		3.0	ns
t_{PTTS}	Product term 3-state delay		4.5		3.5		5.0	ns
Internal Register and Combinatorial delays								
t_{PDI}	Combinatorial logic propagation delay		0.5		1.0		3.0	ns
t_{SUI}	Register setup time	1.5		2.5		3.5		ns
t_{HI}	Register hold time	3.0		3.5		4.5		ns
t_{COI}	Register clock to output valid time		0.5		0.5		0.5	ns
t_{AOI}	Register async. S/R to output delay		6.5		7.0		8.0	ns
t_{RAI}	Register async. S/R recovery before clock	7.5		10.0		10.0		ns
t_{LOGI}	Internal logic delay		2.0		2.5		3.0	ns
t_{LOGILP}	Internal low power logic delay		10.0		11.0		11.5	ns
Feedback Delays								
t_F	FastCONNECT matrix feedback delay		8.0		9.5		11.0	ns
t_{LF}	Function Block local feedback delay		4.0		3.5		3.5	ns
Time Adders								
t_{PTA}[3]	Incremental Product Term Allocator delay		1.0		1.0		1.0	ns
t_{SLEW}	Slew-rate limited delay		4.0		4.5		5.0	ns

Note: 3. t_{PTA} is multiplied by the span of the function as defined in the family data sheet.

XC95144 I/O Pins

Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
1	1	–	–	25	429	
1	2	11	13	18	426	
1	3	12	14	19	423	
1	4	–	–	27	420	
1	5	13	15	21	417	
1	6	14	16	22	414	
1	7	–	–	32	411	
1	8	15	17	23	408	
1	9	16	18	24	405	
1	10	–	–	34	402	
1	11	17	19	26	399	
1	12	18	20	28	396	
1	13	–	–	38	393	
1	14	19	21	29	390	
1	15	20	22	30	387	
1	16	–	–	39	384	
1	17	22	24	33	381	[1]
1	18	–	–	–	378	
2	1	–	–	158	375	
2	2	99	1	159	372	[1]
2	3	–	–	3	369	
2	4	–	–	5	366	
2	5	1	3	2	363	[1]
2	6	2	4	4	360	[1]
2	7	–	–	7	357	
2	8	3	5	6	354	[1]
2	9	4	6	8	351	[1]
2	10	–	–	9	348	
2	11	6	8	11	345	
2	12	7	9	12	342	
2	13	–	–	14	339	
2	14	8	10	13	336	
2	15	9	11	15	333	
2	16	–	–	16	330	
2	17	10	12	17	327	
2	18	–	–	–	324	

Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
3	1	–	–	43	321	
3	2	23	25	35	318	[1]
3	3	–	–	45	315	
3	4	–	–	48	312	
3	5	24	26	36	309	
3	6	25	27	37	306	
3	7	–	–	50	303	
3	8	27	29	42	300	[1]
3	9	28	30	44	297	
3	10	–	–	52	294	
3	11	29	31	47	291	
3	12	30	32	49	288	
3	13	–	–	53	285	
3	14	32	34	54	282	
3	15	33	35	56	279	
3	16	–	–	55	276	
3	17	34	36	57	273	
3	18	–	–	–	270	
4	1	–	–	132	267	
4	2	87	89	140	264	
4	3	–	–	147	261	
4	4	–	–	149	258	
4	5	89	91	142	255	
4	6	90	92	143	252	
4	7	–	–	150	249	
4	8	91	93	144	246	
4	9	92	94	145	243	
4	10	–	–	151	240	
4	11	93	95	146	237	
4	12	94	96	148	234	
4	13	–	–	153	231	
4	14	95	97	152	228	
4	15	96	98	154	225	
4	16	–	–	155	222	
4	17	97	99	156	219	
4	18	–	–	–	216	

Notes: [1] Global control pin.
Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

XC95144 I/O Pins (continued)

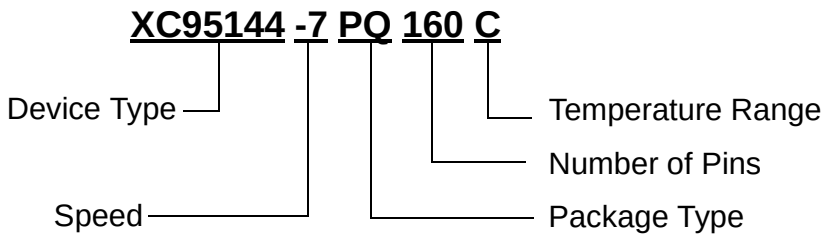
Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
5	1	–	–	65	213	
5	2	35	37	58	210	
5	3	–	–	66	207	
5	4	–	–	67	204	
5	5	36	38	59	201	
5	6	37	39	60	198	
5	7	–	–	74	195	
5	8	39	41	62	192	
5	9	40	42	63	189	
5	10	–	–	76	186	
5	11	41	43	64	183	
5	12	42	44	68	180	
5	13	–	–	78	177	
5	14	43	45	69	174	
5	15	46	48	72	171	
5	16	–	–	83	168	
5	17	49	51	77	165	
5	18	–	–	–	162	
6	1	–	–	–	159	
6	2	74	76	117	156	
6	3	–	–	119	153	
6	4	–	–	123	150	
6	5	76	78	122	147	
6	6	77	79	124	144	
6	7	–	–	125	141	
6	8	78	80	126	138	
6	9	79	81	129	135	
6	10	–	–	128	132	
6	11	80	82	133	129	
6	12	81	83	134	126	
6	13	–	–	130	123	
6	14	82	84	135	120	
6	15	85	87	138	117	
6	16	–	–	131	114	
6	17	86	88	139	111	
6	18	–	–	–	108	

Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
7	1	–	–	–	105	
7	2	50	52	79	102	
7	3	–	–	84	99	
7	4	–	–	85	96	
7	5	52	54	82	93	
7	6	53	55	86	90	
7	7	–	–	87	87	
7	8	54	56	88	84	
7	9	55	57	90	81	
7	10	–	–	89	78	
7	11	56	58	92	75	
7	12	58	60	95	72	
7	13	–	–	91	69	
7	14	59	61	96	66	
7	15	60	62	97	63	
7	16	–	–	93	60	
7	17	61	63	98	57	
7	18	–	–	–	54	
8	1	–	–	–	51	
8	2	63	65	101	48	
8	3	–	–	105	45	
8	4	–	–	107	42	
8	5	64	66	102	39	
8	6	65	67	103	36	
8	7	–	–	109	33	
8	8	66	68	104	30	
8	9	67	69	106	27	
8	10	–	–	112	24	
8	11	68	70	108	21	
8	12	70	72	111	18	
8	13	–	–	114	15	
8	14	71	73	113	12	
8	15	72	74	115	9	
8	16	–	–	118	6	
8	17	73	75	116	3	
8	18	–	–	–	0	

XC95144 Global, JTAG and Power Pins

Pin Type	TQ100	PQ100	PQ160
I/O/GCK1	22	24	33
I/O/GCK2	23	25	35
I/O/GCK3	27	29	42
I/O/GTS1	3	5	6
I/O/GTS2	4	6	8
I/O/GTS3	1	3	2
I/O/GTS4	2	4	4
I/O/GSR	99	1	159
TCK	48	50	75
TDI	45	47	71
TDO	83	85	136
TMS	47	49	73
V_{CCINT} 5 V	5, 57, 98	7, 59, 100	10, 46, 94, 157
V_{CCIO} 3.3 V/5 V	26, 38, 51, 88	28, 40, 53, 90	1, 41, 61, 81, 121, 141
GND	100, 21, 31, 44, 62, 69, 75, 84	2, 23, 33, 46, 64, 71, 77, 86	20, 31, 40, 51, 70, 80, 99, 100, 110, 120, 127, 137, 160
No Connects	–	–	–

Ordering Information



Speed Options

-15 15 ns pin-to-pin delay
-10 10 ns pin-to-pin delay
-7 7 ns pin-to-pin delay

Packaging Options

PQ100 100-Pin Plastic Quad Flat Pack (PQFP)
TQ100 100-Pin Very Thin Quad Flat Pack (TQFP)
PQ160 160-Pin Plastic Quad Flat Pack (PQFP)

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	–40°C to 85°C

Component Availability

Pins		100		160
Type		Plastic PQFP	Plastic TQFP	Plastic PQFP
Code		PQ100	TQ100	PQ160
XC95144	–15	C,I	C,I	C,I
	–10	C,I	C,I	C,I
	–7	C	C	C

C = Commercial = 0°C to +70°C I = Industrial = –40°C to +85°C

Revision Control

Date	Revision
12/04/98	Update AC characteristics and internal parameters.