YAMAHA LSI

YGV610B

CPDC (Color Panel Display Controller)

■ OUTLINE

The CPDC is a display controller for various STN liquid crystal panel displays.
Because it is VRAM address compatible with the IBM-PC, conventional screen data can be displayed unchanged.
A color lookup table and gray-scale pattern table are provided. Up to 512 colors (up to 256 colors can be displayed simultaneously) can be displayed on a color STN liquid crystal display panel and a display system with such advanced functions as display of up to 15 gray-scales on a monochrome LCD can be easily built.

■ FEATURES

Display functions

- One-screen color and monochrome STN liquid crystal display panels from 128 × 128 to 640 × 240 dots can be driven.
- A two-screen monochrome STN liquid crystal display panel of up to 640 × 480 dots can be driven.
- Data of each dot can be selected from among 2, 4, and 8 bits (4, 16, and 256 colors display). (1-screen LCD output)
- Data of each dot can be selected from 1 and 2 bits (2 and 4 gray-scales display). (2-screen LCD output)
- Built-in color lookup table for simultaneous display of 4/16 colors from among 512 colors.
- Built-in gray-scale pattern table capable of displaying up to 512 colors for color panel use and up to 15 gray-scales for monochrome panel use.

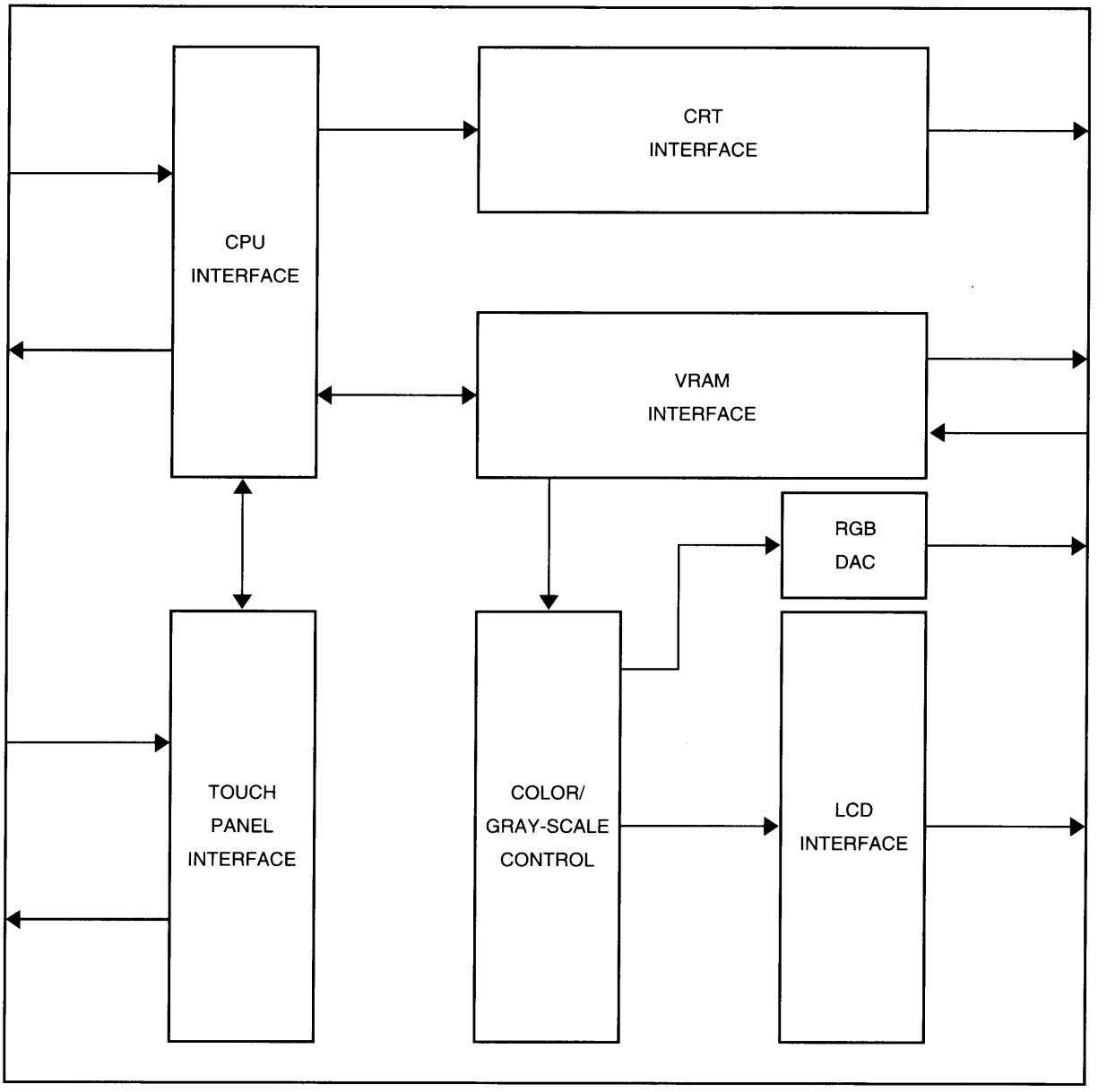
Others

- DRAM with a 4/8-bit bus configuration can be used.
  (High-speed page mode DRAM from 256kb to 8Mb can be accessed)
- VRAM address compatible with IBM-PC CGA and VGA.
- Supports low-power modes (standby mode, power down mode).
- In the standby mode, DRAM refresh operation is possible in a "$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$" mode.
- Can be connected to various LCD.
  (Supports 1-screen monochrome LCD panel, 2-screen monochrome LCD panel, and 1-screen color LCD panel (4-bit, 8-bit data output))
- Built-in DAC with 3-bit R, G and B inputs. Output to a CRT is also possible.
- Built-in touch panel interface circuit.
- 100-pin plastic QFP.
- Power supply can be selected from 5.0V and 3.3V.

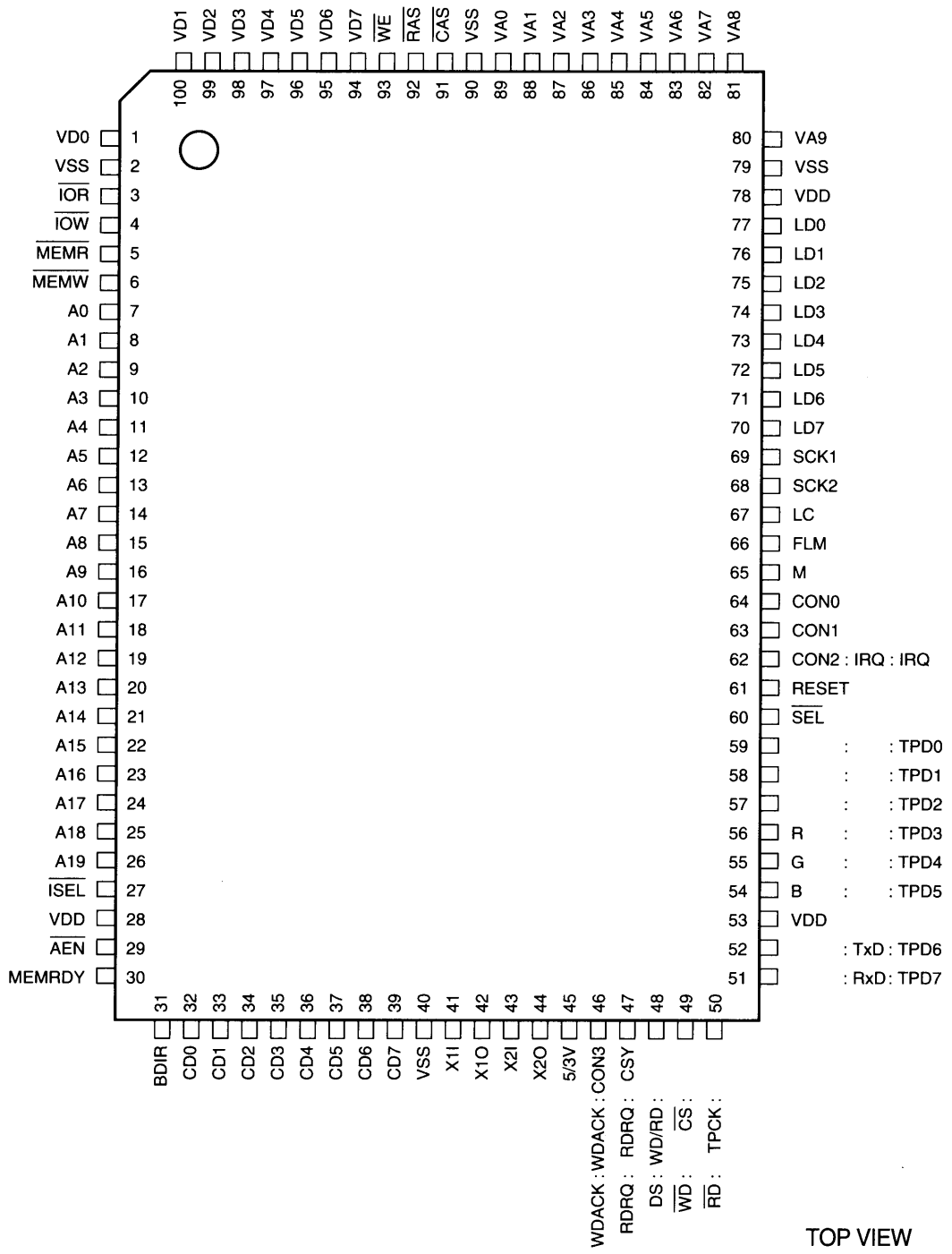
YAMAHA CORPORATION

YGV610B CATALOG
CATALOG No.: LSI-4GV610B2
1997. 4

■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



Outside: Touch panel i/f parallel port mode
Center : Touch panel i/f serial port mode
Inside : DAC output mode

Note) Blank columns from pins 48 to 59 are function-less input pins. Pull them up or down.

■ PIN FUNCTIONS

1) CPU interface

- CD[7:0](I/O)
  CPU 8-bit bi-directional data bus.
- A[19:0](I)
  CPU 20-bit address bus.
- BDIR (O)
  CPU data bus output direction.
- $\overline{\text{SEL}}$ (I)
  IBM-PC address compatible mode select.
- $\overline{\text{ISEL}}$ (I)
  I/O register access enable.
- $\overline{\text{AEN}}$ (I)
  I/O select address enable.
- $\overline{\text{IOW}}$ (I)
  I/O register write request.
- $\overline{\text{IOR}}$ (I)
  I/O register read request.
- $\overline{\text{MEMW}}$ (I)
  VRAM write request.
- $\overline{\text{MEMR}}$ (I)
  VRAM read request.
- MEMRDY (0:3-state)
  VRAM Access Ready signal.

2) VRAM interface

- VA[9:0](O)
  VRAM address bus.
- VD[7:0](I/O)
  VRAM data bus.
- $\overline{\text{RAS}}$ (O)
  Row address strobe signal.
- $\overline{\text{CAS}}$ (O)
  Column address strobe signal.
- $\overline{\text{WE}}$ (O)
  Write enable signal.

3) LCD interface

- LD[7:0](O)
  LCD data bus.
- FLM (O)
  Scan start-up signal.
- LC (O)
  Display data latch clock.
- SCK1,2 (O)
  Display data shift clocks 1 and 2.
- M (O)
  LCD drive signal alternation.

4) Others

- RESET (I)
  Power-on reset input.
- CON[1:0](O)
  External control register output.
- X1I (I)
  Clock oscillation inverter input 1.
- X1O (O)
  Clock oscillation inverter output 1.
- X2I (I)
  Clock oscillation inverter input 2.
- X2O (O)
  Clock oscillation inverter output 2.
- 5/3V (I)
  Power supply voltage selection pin .

5) Touch panel interface pins

The function of the following pins depends on the register setting value.
In the initial state immediately after power-on, the DAC output mode is selected.
Pull unused input pins up or down.

(1) DAC output mode

In this mode, the touch panel interface is not used. (Initial state immediately after power-on)
When 5/3V="H", the CRT interface can be used.

- CON[3:2](O)
  When the CPDC is used in the DAC output mode, two external control register output functions can be added.
- CSY (O)
  When CRT interface was selected in the DAC output mode, this pin becomes the composite synchronizing signal output.
- R.G.B (analog O)
  When CRT interface was selected in the DAC output mode, 3-bit DAC output R. G. B can be used.

(2) Serial port mode

A clock synchronous serial interface circuit for single-chip microcomputer with A/D converter and other touch panel module processing functions can be used.

- WD/RD (I)
  Serial port transmission command input.
- $\overline{CS}$ (I)
  Chip select. When this pin is "L" level, transmission is enabled.
- TPCK (I)
  Serial data transmission clock input.
- TxD (O)
  Serial data output. Outputs LSB-first 8-bit data.
- RxD (I)
  Serial data input.
- IRQ (O)
  Interrupt signal to CPU.

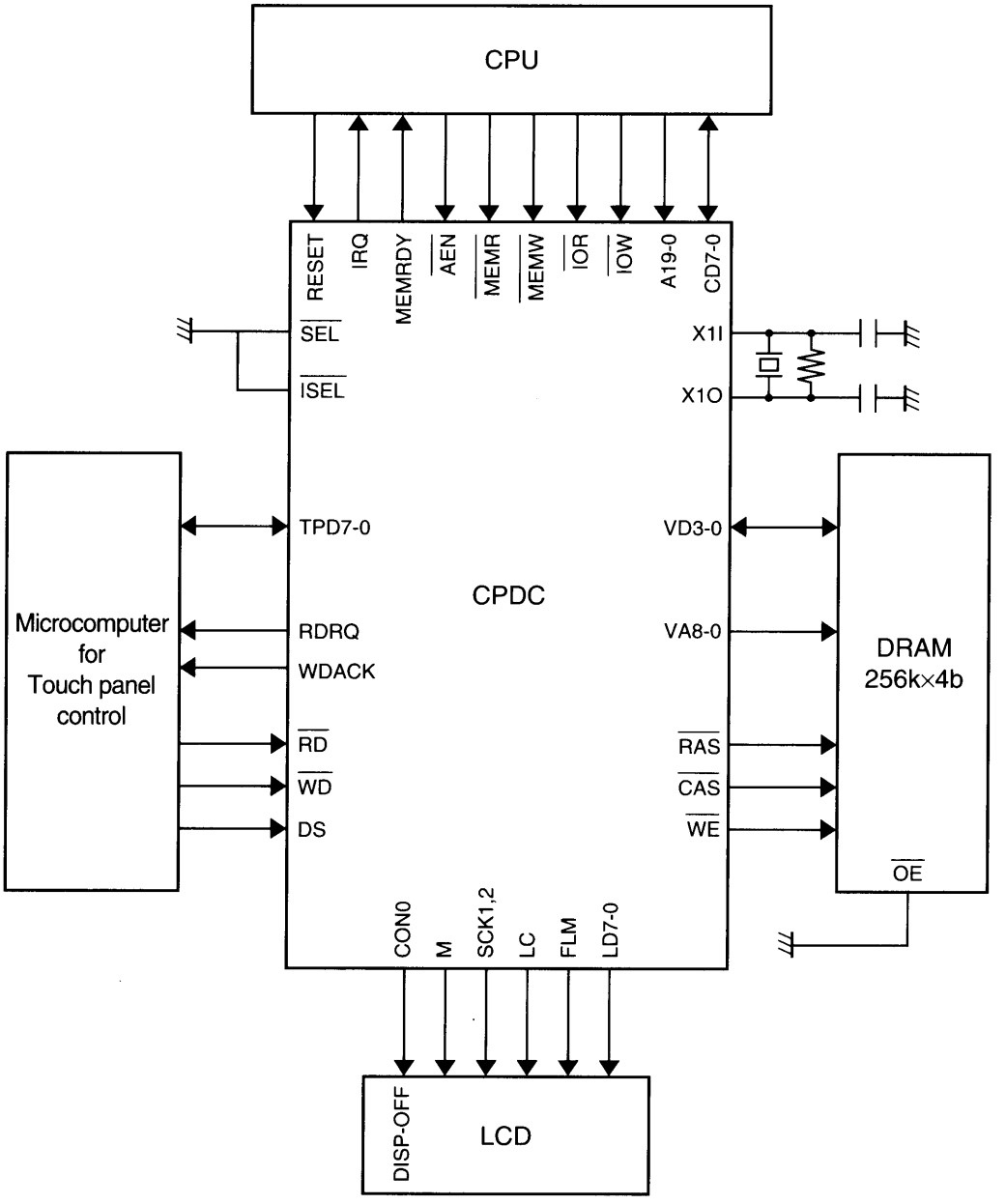
- RDRQ (O)
  CPU to single-chip microcomputer data read request.
- WDACK (O)
  CPU to single-chip microcomputer data write permission.

(3) Parallel port mode

An 8-bit parallel interface circuit for single-chip microcomputer with A/D converter and other touch panel module processing functions can be used.

- TPD[7:0](I/O)
  Parallel data input/output.
- $\overline{RD}$ (I)
  Data read request input.
- $\overline{WD}$ (I)
  Data write strobe input.
- DS (I)
  Selects the contents to be read by the single-chip microcomputer.
- IRQ (O)
  Interrupt signal to CPU.
- RDRQ (O)
  CPU to single-chip microcomputer data read request.
- WDACK (O)
  CPU to single-chip microcomputer data write permission.

■ SYSTEM CONFIGURATION EXAMPLE



■ ELECTRICAL CHARACTERISTICS

• Absolute maximum ratings

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{DD}	–0.5	+7.0	V
Input terminal voltage	V_I	–0.5	VDD+0.5	V
Output terminal voltage	V_O	–0.5	VDD+0.5	V
Ambient operating temperature	T_{OP}	0	+70	°C
Storage temperature	Tstg	–50	+125	°C

Vss=0.0V Base

• Recommended operating conditions

Supply voltage	5V system	+5.0V±5%
	3V system	3.3V±0.3V
Ambient operating temperature	0~+70°C	

• Electrical characteristics under recommended operating conditions

- DC characteristics

① 5V system

V_{DD} = +5.0V±5%

T_{OP} = 0~+70°C

Item	Symbol	Condition	Min.	Max.	Unit
High level output voltage (for TTL driving)	V_{OH}	I_{OH}=–0.4mA	2.7		V
Low level output voltage (for TTL driving)	V_{OL}	I_{OL}=2.0mA		0.4	V
High level output voltage (for CMOS driving)	V_{OH}	I_{OH}=–100µA	V_{DD}–0.4		V
Low level output voltage (for CMOS driving)	V_{OL}	I_{OL}=100µA		0.4	V
High level input voltage[1)]	V_{IH}		2.2		V
Low level input voltage[1)]	V_{IL}			0.8	V
High level input voltage[2)]	V_{IH}		0.7V_{DD}		V
Low level input voltage[2)]	V_{IL}			0.3V_{DD}	V
High level input voltage[3)]	V_{IH}		0.7V_{DD}		V
Low level input voltage[3)]	V_{IL}			0.8	V
Input leakage current	I_L		–10	10	µA
Off state leakage current[4)]	I_{LZ}		–10	10	µA
Power consumption (normal operation)	I_{DD}	V_{DD}=5.25V		35	mA
Power consumption (standby mode)	I_{DD}	V_{DD}=5.25V		12	mA
Power consumption (LCD driving power down mode)[5)]	I_{DD}	V_{DD}=5.25V		100	µA

Notes 1) Except 5/3V, X1I, X2I, and $\overline{SEL}$ input pins.

2) X1I, and X2I pins.

3) 5/3V, and $\overline{SEL}$ pins.

4) When CD7-0, VD7-0, and TPD7-0 are in the input state and MEMRDY is in the high-impedance state.

5) When the LCD is operated (the levels of input pins are fixed to the V_{DD} and Vss levels.)

② 3V system
V_{DD} = +3.3V±0.3V
T_{OP} = 0~+70°C

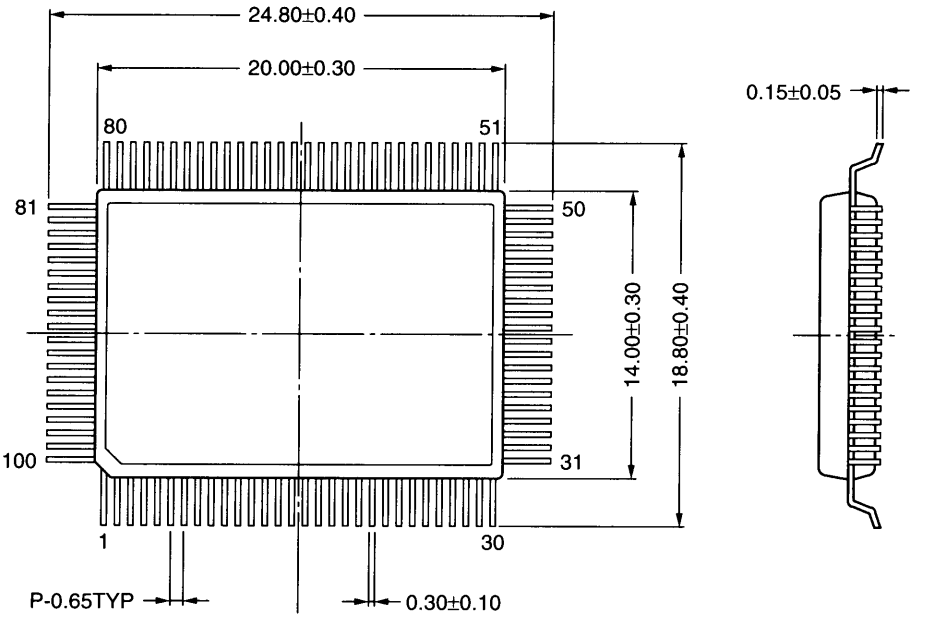
Item	Symbol	Condition	Min.	Max.	Unit
High level output voltage (for TTL driving)	V_{OH}	I_{OH}=–0.2mA	2.4		V
Low level output voltage (for TTL driving)	V_{OL}	I_{OL}=1.0mA		0.4	V
High level output voltage (for CMOS driving)	V_{OH}	I_{OH}=–100µA	V_{DD}–0.4		V
Low level output voltage (for CMOS driving)	V_{OL}	I_{OL}=100µA		0.4	V
High level input voltage[1)]	V_{IH}		2.0		V
Low level input voltage[1)]	V_{IL}			0.8	V
High level input voltage[2)]	V_{IH}		0.7V_{DD}		V
Low level input voltage[2)]	V_{IL}			0.3V_{DD}	V
High level input voltage[3)]	V_{IH}		0.7V_{DD}		V
Low level input voltage[3)]	V_{IL}			0.8	V
Input leakage current	I_L		–10	10	µA
Off state leakage current[4)]	I_{LZ}		–10	10	µA
Power consumption (normal operation)	I_{DD}	V_{DD}=3.6V		15	mA
Power consumption (standby mode)	I_{DD}	V_{DD}=3.6V		6	mA
Power consumption (power down mode)[5)]	I_{DD}	V_{DD}=3.6V		50	µA

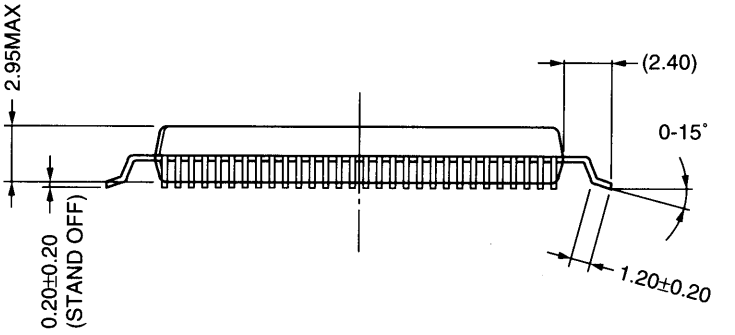
Notes 1) Except 5/3V, X1I, X2I, and $\overline{SEL}$ input pins.
2) X1I, and X2I pins.
3) 5/3V, and $\overline{SEL}$ pins.
4) When CD7-0, VD7-0, and TPD7-0 are in the input state and MEMRDY is in the high-impedance state.
5) When the LCD is operated (the levels of input pins are fixed to the V_{DD} and Vss levels.)

- Terminal capacitance

Item	Symbol	Condition	Min.	Max.	Unit
Input terminal capacity	C_I			8	pF
Output terminal capacity	C_O	No load		10	pF
Input/output terminal capacity	C_{IO}	No load		12	pF

■ EXTERNAL DIMENSIONS





UNIT : mm

Note : The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

■ MEMO

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