
YAMAHA[®] LSI

YM7128B

Surround Processor
(SP2)

■ OUTLINE

This is an LSI which has quality digital surround sound capabilities realized by Yamaha's digital audio technology. The LSI has built-in A/D and D/A converters which enable digital surround sound processing for analog input/output. Its eight digital delay lines may provide delay time of up to 100 msec. for each, and digital adding up of delay line signals for two-channel output assures a wide range of application.

■ FEATURES

- The built-in RAM realizes digital delay time of 100 msec.* at the maximum.
- Feedback loop can be constructed for reverberation.
- Various surround effect can be obtained by controlling this LSI with serial data from microprocessor.
- Digital attenuator is built in for surround sound volume control.
- Sampling frequency is 23.6 kHz*, and 14 bit floating A/D converter is built in.
- Two-times oversampling digital filter and 14 bit floating D/A converter are built in.
- 16 pin DIP, 24 pin SOP package, silicone gate CMOS 5V power supply.

Note) When XI clock frequency is 7.16 MHz (304 fs is required for XI clock).

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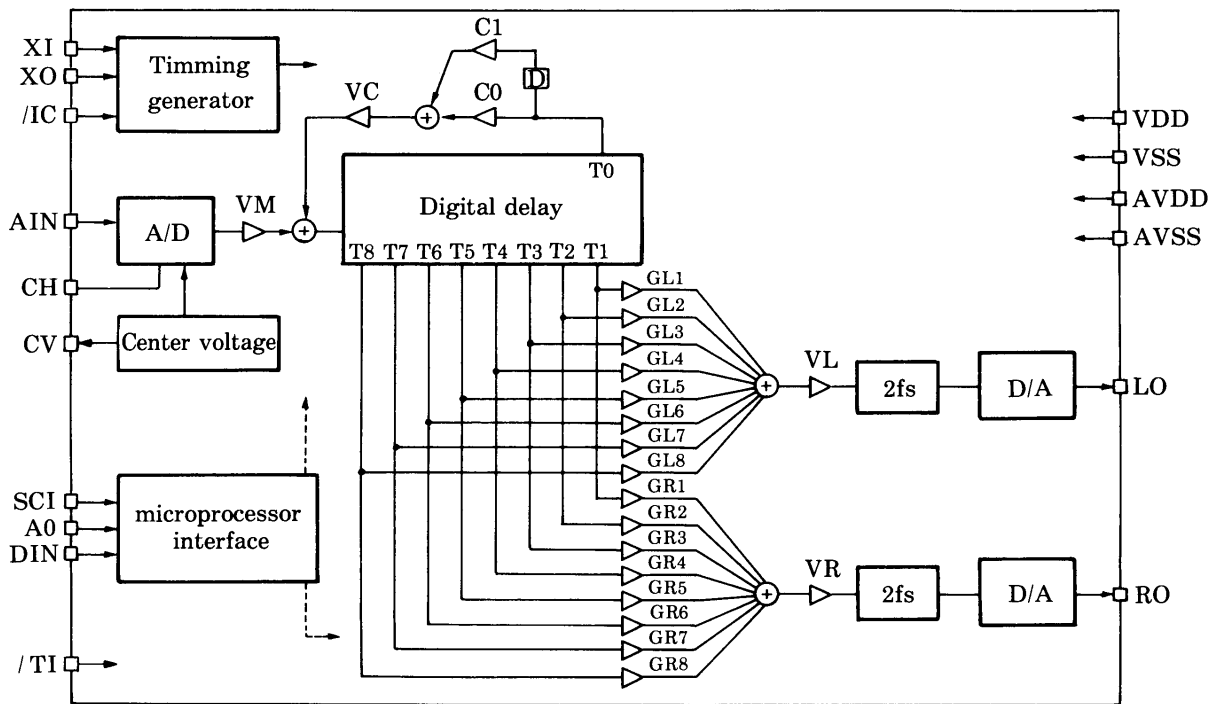
YM7128B CATALOG
CATALOG No. : LSI-2171284
1992.11

■ PIN DESCRIPTIONS

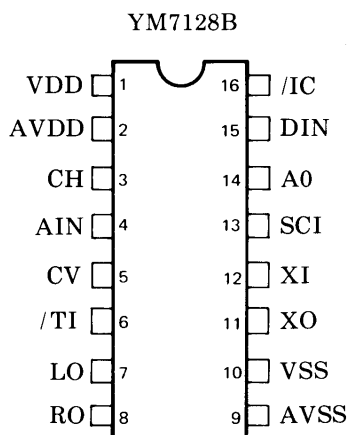
Name	I/O	Function
VDD	—	Digital +5V power supply
AVDD	—	Analog +5V power supply
CH	O	Sample/hold capacitor terminal
AIN	I	Analog signal input
CV	O	Center voltage of A/D
/TI	I+	Test terminal (without connection)
LO	O	L channel, analog out
RO	O	R channel, analog out
AVSS	—	Analog ground
VSS	—	Digital ground
XO	O	X'tal oscillator terminal (7.16 MHz typ.)
XI	I	
SCI	I	Bit clock for microprocessor interface
A0	I	Word clock for microprocessor interface
DIN	I	Serial data for microprocessor interface
/IC	I+	Initial clear terminal

+; pulled up

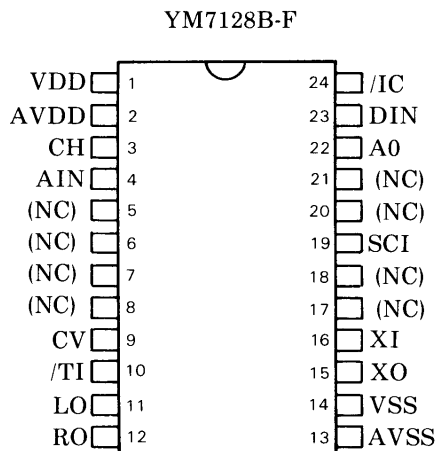
■ BLOCK DIAGRAM



■ PIN CONFIGURATIONS



TOP VIEW



TOP VIEW

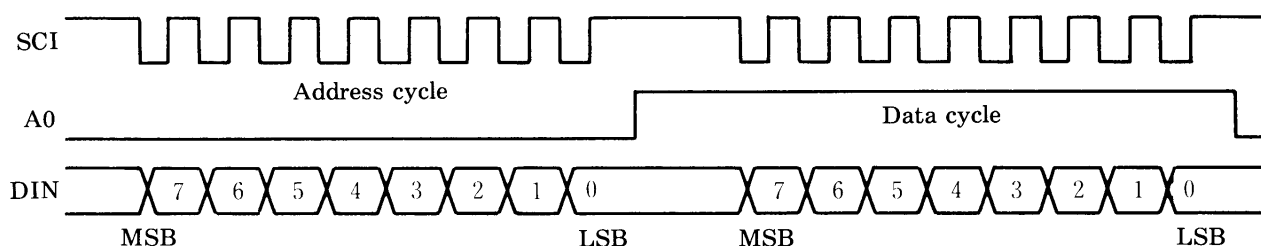
■ FUNCTION DESCRIPTION

As shown in the block diagram, analog signal input at AIN terminal are converted to 14 bit digital signal with the sampling frequency of 23.6 kHz using 14 bit floating type A/D converter, and then attenuated by the digital attenuator VM. Tap T0 output of digital delay passes through first order FIR type low pass filter and attenuated by VC. These signals are added before they are input to digital delay. Digital delay has nine output taps and tap positions can be switched by the registers T0 to T8. Outputs of eight taps from T1 to T8 are attenuated and added for each channel with the digital attenuator from GL1 to GL8 and GR1 to GR8 respectively, and attenuated by digital attenuator VL or VR to be input to two-times oversampling digital filter. Since this filter attenuates aliasing noise, it reduces the burden on external analog low pass filter. Digital input to D/A converter shall be with doubled value, which is 47.1 kHz sampling rate.

■ MICROPROCESSOR INTERFACE

Digital attenuation value, delay time and FIR type low pass filter coefficients are all set by writing data into registers.

With A0 = "L", 8 bit address data are sent synchronizing with SCI. At the rising edge of A0, register address is taken in. With A0 = "H", 8 bit data are sent synchronizing with SCI, then register data are changed at the falling edge of A0.



- At the time of initial clear, VM, VC, VL and VR registers are reset to 0. Other register values are not fixed.

■ REGISTER MAP

Address (HEX)	Data					Function
	7	6	5	4	3 2 1 0	
00	x	x			GL1	Lch Tap attenuation value (bit 5; sign)
01	x	x			GL2	
02	x	x			GL3	
03	x	x			GL4	
04	x	x			GL5	
05	x	x			GL6	
06	x	x			GL7	
07	x	x			GL8	
08	x	x			GR1	Rch Tap attenuation value (bit 5; sign)
09	x	x			GR2	
0A	x	x			GR3	
0B	x	x			GR4	
0C	x	x			GR5	
0D	x	x			GR6	
0E	x	x			GR7	
0F	x	x			GR8	

Address (HEX)	Data					Function
	7	6	5	4	3 2 1 0	
10	x	x			VM	Attenuation value (bit 5; sign)
11	x	x			VC	
12	x	x			VL	
13	x	x			VR	
14	x	x			C0	FIR coefficient
15	x	x			C1	
16	x	x	x		T0	Tap position
17	x	x	x		T1	
18	x	x	x		T2	
19	x	x	x		T3	
1A	x	x	x		T4	
1B	x	x	x		T5	
1C	x	x	x		T6	
1D	x	x	x		T7	
1E	x	x	x		T8	

Note 1) x; Don't Care

Note 2) Don't write to the other address

■ REGISTER DATA DESCRIPTION

(1) Attenuation value setting (GL1 to GL8, GR1 to GR8, VM, VC, VL, VR)

- Output polarity (bit 5)

When bit 5 = "1": Output signal is in phase with input signal.

When bit 5 = "0": Output signal is reversed phase with input signal.

- Attenuation value (bit 4–0)

Level (dB)	Data					(HEX)
	4	3	2	1	0	
0	1	1	1	1	1	1F
-2	1	1	1	1	0	1E
-4	1	1	1	0	1	1D
-6	1	1	1	0	0	1C
-8	1	1	0	1	1	1B
-10	1	1	0	1	0	1A
-12	1	1	0	0	1	19
-14	1	1	0	0	0	18
-16	1	0	1	1	1	17
-18	1	0	1	1	0	16
-20	1	0	1	0	1	15
-22	1	0	1	0	0	14
-24	1	0	0	1	1	13
-26	1	0	0	1	0	12
-28	1	0	0	0	1	11
-30	1	0	0	0	0	10

Level (dB)	Data					(HEX)
	4	3	2	1	0	
-32	0	1	1	1	1	0F
-34	0	1	1	1	0	0E
-36	0	1	1	0	1	0D
-38	0	1	1	0	0	0C
-40	0	1	0	1	1	0B
-42	0	1	0	1	0	0A
-44	0	1	0	0	1	09
-46	0	1	0	0	0	08
-48	0	0	1	1	1	07
-50	0	0	1	1	0	06
-52	0	0	1	0	1	05
-54	0	0	1	0	0	04
-56	0	0	0	1	1	03
-58	0	0	0	1	0	02
-60	0	0	0	0	1	01
-∞	0	0	0	0	0	00

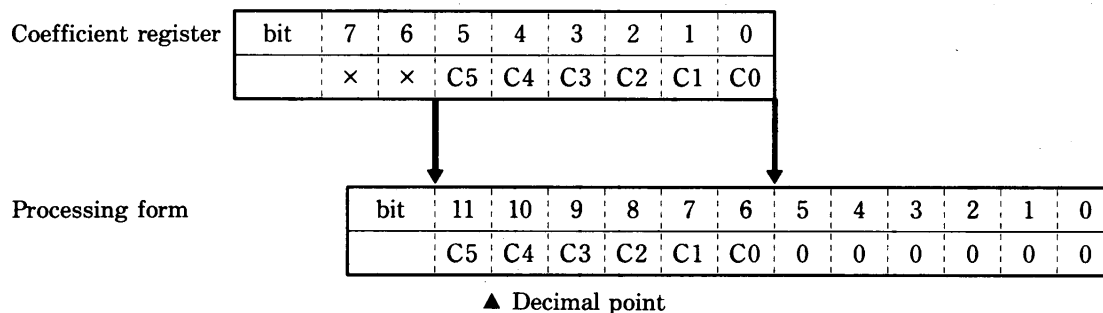
(2) Delay time setting (T0 to T8) (XI = 7.16 MHz)

Delay time (ms)	Data		
	4	3	2 1 0 (HEX)
0.0	0	0	00
3.2	0	0	01
6.5	0	0	02
9.7	0	0	03
12.9	0	0	04
16.1	0	0	05
19.3	0	0	06
22.6	0	0	07
25.8	0	1	08
29.0	0	1	09
32.3	0	1	0A
35.5	0	1	0B
38.7	0	1	0C
41.9	0	1	0D
45.2	0	1	0E
48.4	0	1	0F

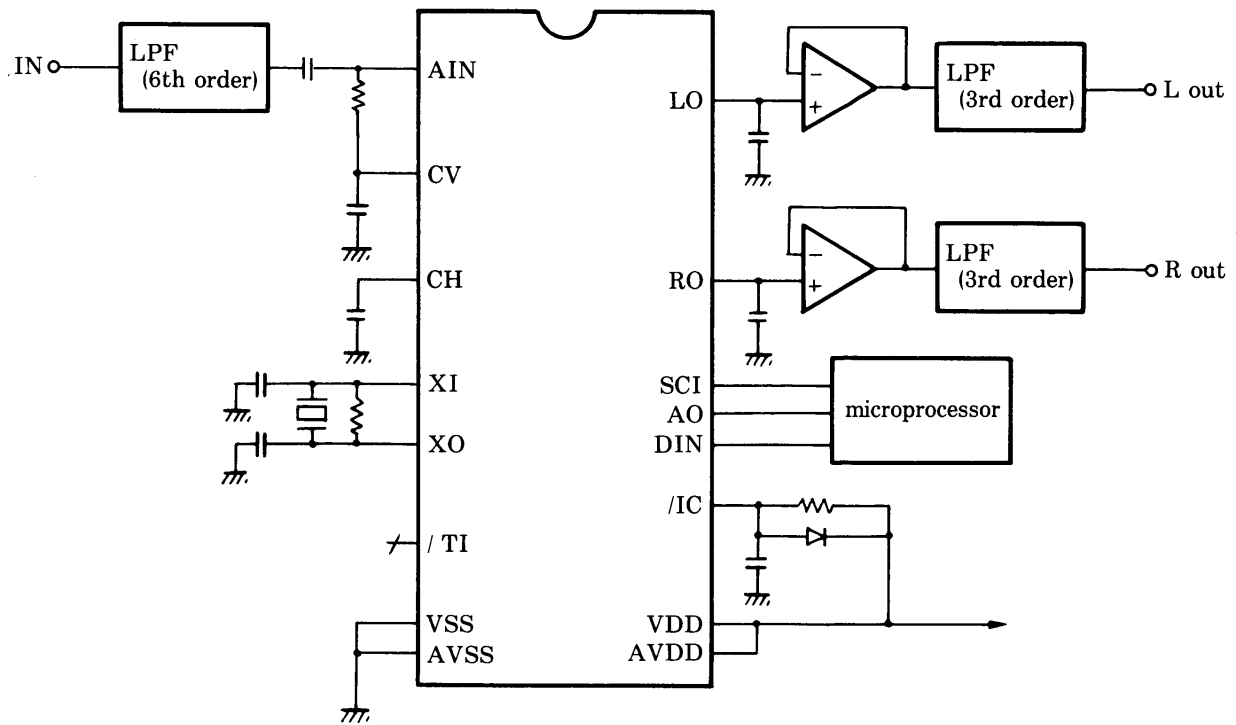
Delay time (ms)	Data		
	4	3	2 1 0 (HEX)
51.6	1	0	10
54.9	1	0	11
58.1	1	0	12
61.3	1	0	13
64.5	1	0	14
67.8	1	0	15
71.0	1	0	16
74.2	1	0	17
77.4	1	1	18
80.7	1	1	19
83.9	1	1	1A
87.1	1	1	1B
90.4	1	1	1C
93.6	1	1	1D
96.8	1	1	1E
100.0	1	1	1F

(3) FIR Low Pass Filter coefficient setting (C0, C1).

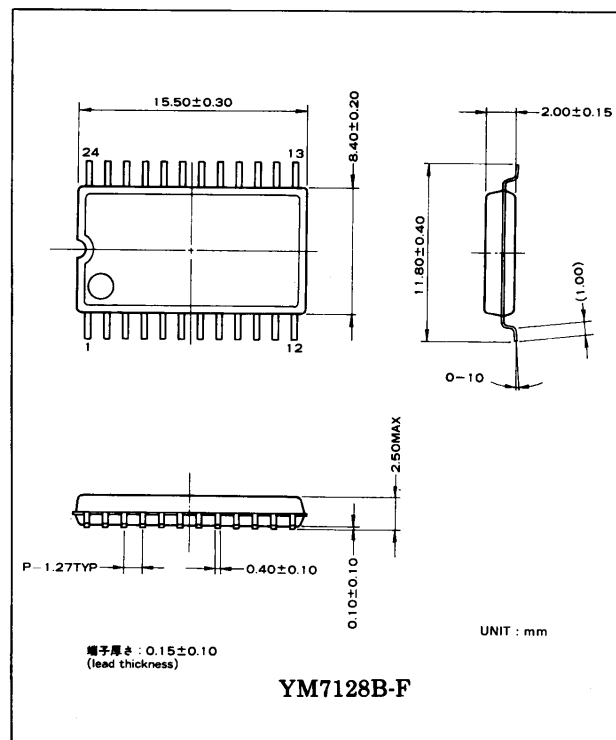
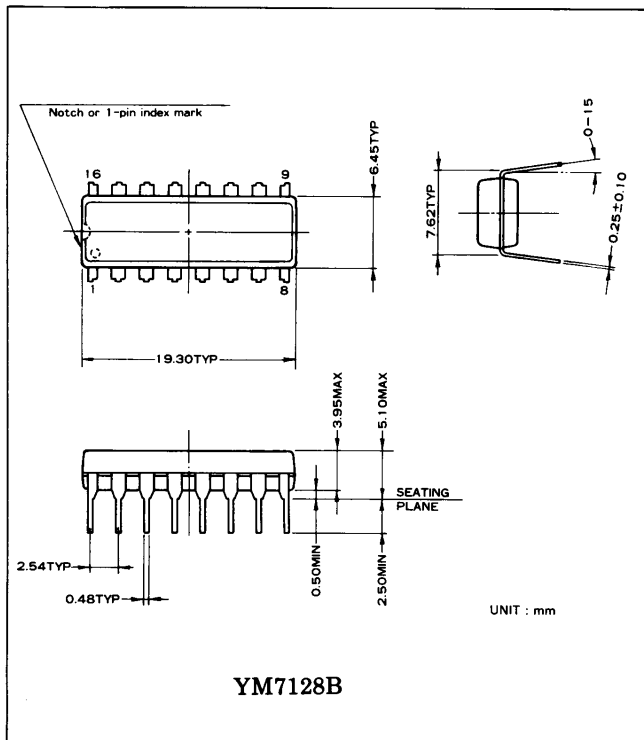
The lower 6 bits of coefficient register are used as the upper 6 bits of 12 bit 2's complement data actually processed inside.



■ SYSTEM BLOCK DIAGRAM



■ EXTERNAL DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

● Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 ~ +7.0	V
Operating temperature	Top	-20 ~ +85	°C
Storage temperature	Tstg	-50 ~ +125	°C

● Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	4.75	5.0	5.25	V
Operating temperature	Top	0	25	70	°C

● DC characteristics (Conditions: Ta = 25°C, VDD = 5.0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	IDD				50	mA
High-level input voltage (1)	VIH1		2.0			V *1
Low-level input voltage (1)	VIL1				0.8	V *1
High-level input voltage (2)	VIH2		4.0			V *2
Low-level input voltage (2)	VIL2				0.8	V *2
High-level output voltage	VOH	IOH = -0.4mA	4.0			V
Low-level output voltage	VOL	IOL = 0.2mA			0.4	V
Input leakage current	IIL	VI = 0 ~ 5V	-10		10	μA
Input capacitance	CI			5.0	12.0	pF
Output capacitance	CO				10.0	pF

Note 1: Applicable to the input terminals except XI

Note 2: Applicable to XI terminal

● AC characteristics (Conditions: Ta = 25°C, VDD = 5.0V)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
XI	Input frequency	fc	3.6	7.16	8.0	MHz
	Duty		40	50	60	%
	Rise time	TCR			50	ns
	Fall time	TCF			50	ns
SCI	Input frequency	fs			fc/8	MHz
	On-off time	TS	600			ns
	Rise time	TSR			200	ns
	Fall time	TSF			200	ns

● **ANALOG characteristics** (Conditions: $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$)

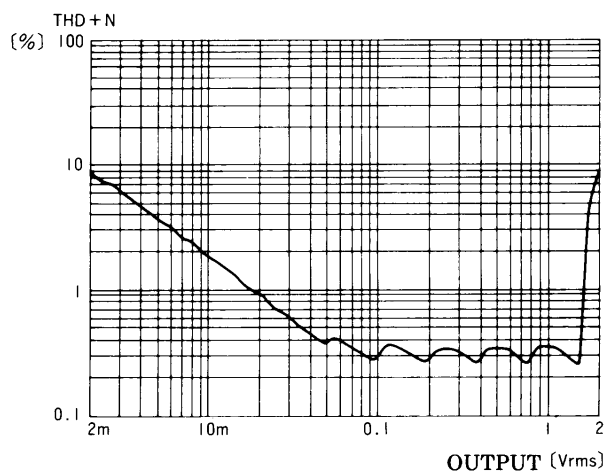
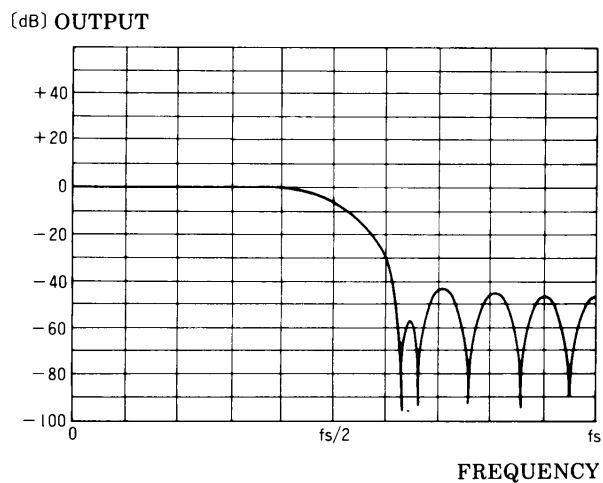
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog input voltage	VIA	AIN terminal			4.5	Vp-p
Analog output voltage	VOA	LO, RO terminal			4.5	Vp-p
DC offset voltage	CV			2.5		V
Total harmonic distortion	THD	output voltage 0dB		0.3	0.4	%
		-10dB		0.4	0.5	%
		-20dB		0.4	0.5	%
		-30dB		0.6	0.8	%
S/N	S/N	S = 0dB	75	80		dB

Note) 0dB=1.5Vrms

■ **REFERENCE CHARACTERISTICS**

2 times oversampling filter

Output vs THD + NOISE



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