YAMAHA LSI

YGV613

NVDP
Navigation System VDP

Preliminary

■ OVERVIEW

The YGV613 ("NVDP") is a video display processor suited for automobile navigation systems. The NVDP can provide superimposed displays consisting of map layer, place-name layer, and other application layers. It supports color space conversion by means of its built-in "naviken" format △YUV and YUV422 drawn-data decode function. With head-up function included and LCD connection supported, the NVDP makes a significant contribution to the performance of navigation systems.

The chip's ability to provide full-color display, multilayered display, and high-speed drawing makes it suitable for a variety of other display applications as well. For example, it is appropriate for motion picture display (in conjunction with an MPEG decoder), karaoke and video titler systems with natural pictures or16-color pictures.

In addition to its display clock, an independent system clock can be selected for optimal DRAM access speed, allowing to construct a high-speed drawing system by using low-cost memory.

■ FEATURES

[Display Structure]

- Displays up to three bit-mapped layers (each with 16 simultaneous colors)
- In stead of two 16-color layers, one simultaneous 256-color bit-map layer or natural picture display (about 16 million colors) based on △ YUV format can be displayed.
- YUV422-format natural picture display.
- Includes pattern RAM supporting two sprite displays (16-color/32x32 dot)
- Each sprite display can be set to cross hairs cursor.

[Display Functions]

- Monitor-sync frequency, dot-clock frequency (up to 16MHz) and display resolution can be set by parameters.
- High resolution (horizontal 720 dot x vertical 480 line)
- Two independent smooth scrolling functions (Scroll A/Scroll B)
- North/south head-up display (180° rotation)
- Priority can be set separately for each display.
- Semi-transparent display by color calculation function.
- Built-in 256-word by 19-bit CLUT (6 bits each for R, G, and B, plus 1 YS bit), allowing display color selection from among 260,000 colors.
- Linear RGB output by built-in DAC (8 bits each for R, G, and B)
- Super-imposing by external sync function.

YAMAHA CORPORATION

YGV613 CATALOG
CATALOG No. : LSI-4GV613A0
1996. 5

[Drawing Functions]

- Command types
  - Block transfer (pixel blt; word transfer)
  - Rectangle, dot, polydot, line, polyline, and font drawing.
  - Border-color detection, ~~line drawing up to the border~~.
- Drawing attributes
  - 16 built-in LUTs (lookup tables) for line-pattern settings.
  - 16 built-in LUTs for texture-pattern settings.
  - Setting of drawing clip area and drawing page.
  - Bit masking, Color masking, Logical operations (NOT, AND, OR, EOR, etc.)
  - Selectable transfer direction (Rotation of drawing in 90° increments)
  - Selectable width (1 to 4 dots) for lines and polylines
- Drawing speeds
  - Fill-in: Min. 1/8 VCLK/dot (where 1 VCLK=min. 50ns)
  - Dot write (Read-modified write): Min. 2VCLK/dot
  - (where VCLK refers to clock input at VCKIN)

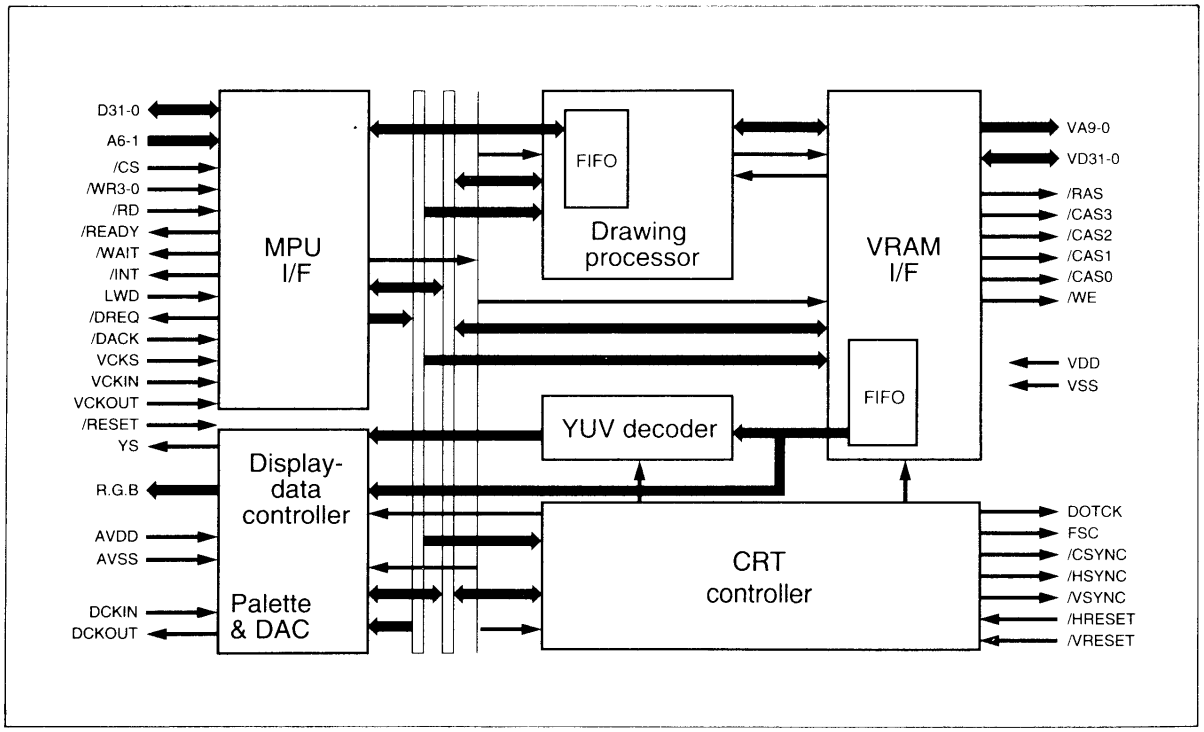
[MPU interface]

- 16-bit or 32-bit asynchronous interface.
- Internal registers mapped to 128-byte I/O space.
- Built-in FIFO memory for drawing data.
- MPU-interrupt function.
- Drawing data DMA transfer by external DMA controller.

[Other features]

- Separate video memory clock can be connected to the DCKIN pin, enabling best matches for the connecting DRAM access speed. This clock is independent from the display clock connected at the DCKIN pin.
- Internal display-data FIFO memory enables high-speed drawing by reducing overhead during accessing of drawing data).
- 144-pin plastic SQFP (CMOS), 5V single power supply.

■ BLOCK DIAGRAM



(1) MPU interface

Asynchronous interface circuit to connect to the general purpose micro processor.

(2) CRT controller

General purpose CRT controller to enable connection to various monitors.

(3) VRAM interface

Interface circuit with DRAM which is connected as a video memory.

(4) Drawing processor

Processor to interpret the drawing command from the MPU and generate the drawing address.

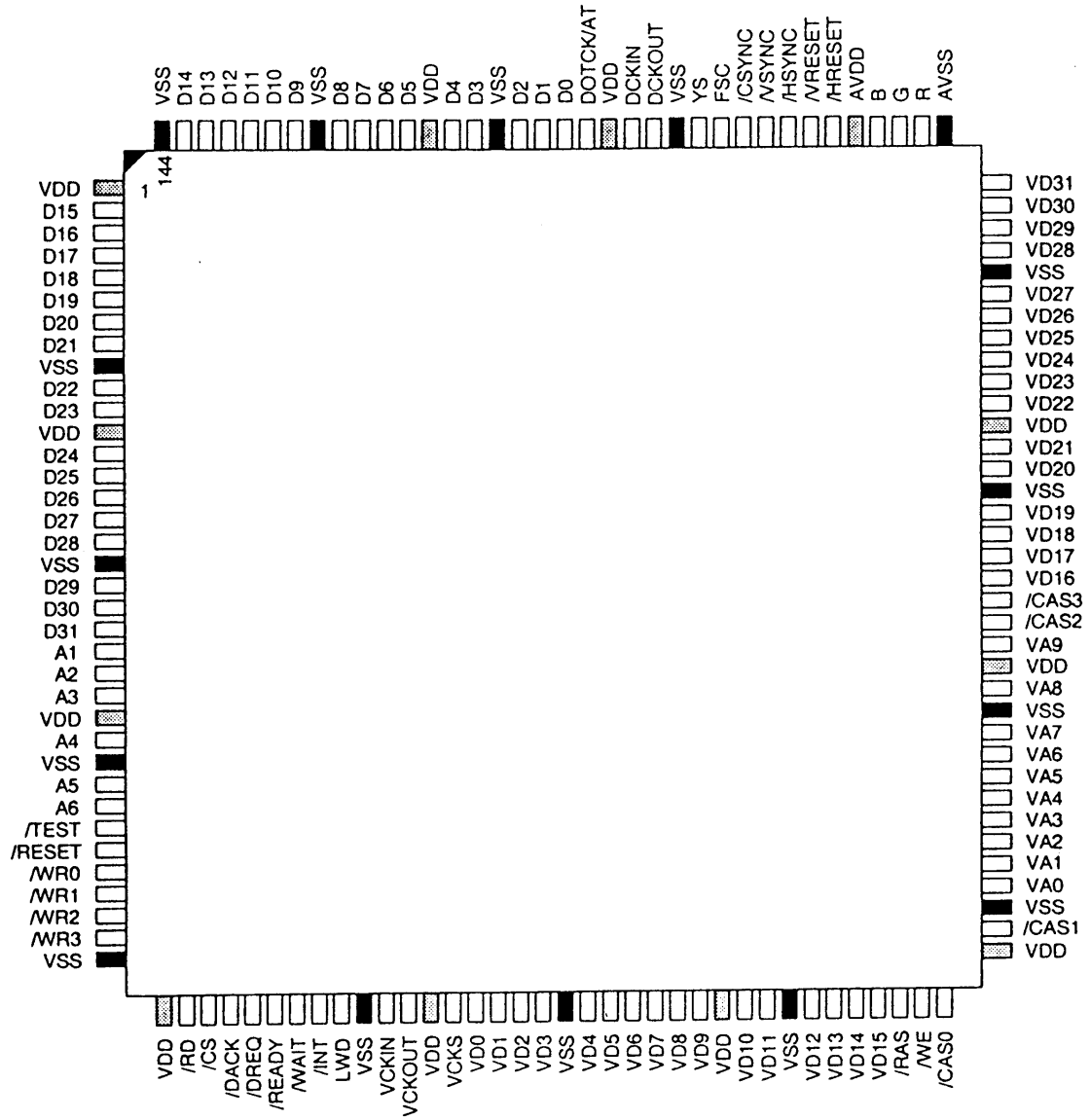
(5) YUV decoder

Reads "naviken" format compressed △YUV data and YUV422 data from video memory, and converts them into serial dot data.

(6) Display data controller

Controller to reconstruct the display screen by overlapping up to 3 display screens according to the priority order.

■ PIN CONFIGURATION



144 SQFP Top View

■ PIN FUNCTION

● System Interface]

D31-0(MPU data bus, input/output)
Data bus to be connected with external general purpose micro processor

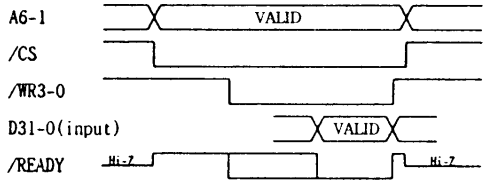
A6-1 (MPU address bus, input)
Address bus to be connected with external general purpose micro processor

/CS (Chip select (low active), input)
Chip select signal input for NVDP internal register access

/WR3-/WR0 (write pulse 3 - 0 (low active), input)
Write access control for NVDP when chip select input is active

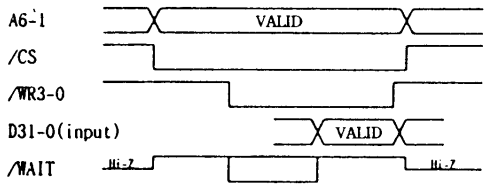
/RD (read pulse (low active), input)
Read access control for NVDP when chip select input is active

/READY (Data ready (low active), 3-state output
Data ready signal output. Use this signal or /WAIT signal depending on the MPU.



/READY output when write access is used

/WAIT (data wait (low active), 3-state output)
Data wait signal output. Use this signal or /READY signal depending on the MPU.



/WAIT output when write access is used

/INT (Interrupt (low active), open drain output)
Interrupt request signal output. Reset by access to internal register.

LWD (MPU data bus width select, input)
To select MPU data bus width select. Usable for 32-bit as well as 16-bit systems

/RESET (Reset (low active), input)
Initial reset signal input. Reset internal settings including registers.

/DREQ (DMA request (low active) output)
Command data request signal output to external DMA controller

/DACK (DMA acknowledge (low active), input)
Command data transfer permit signal input for /DREQ signal from external DMA controller

- **[Video Memory Interface]**

VA9 - VA0 (DRAM address, output)
Address output to the video memory DRAM

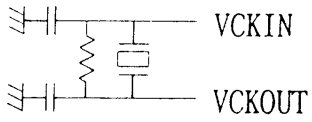
VD31 - VD0 (DRAM data, input/output)
Data bus to the video memory DRAM

/RAS (Row address strobe (low active), output)
DRAM row address strobe signal output

/CAS 3 - 0 (Column address strobe (low active), output)
DRAM column address strobe signal output

/WE (DRAM write enable (low active), output)
DRAM write enable signal output

VCKIN, VCKOUT (XTAL input/output, input/output)
Crystal oscillator connection pin. Input to VCKIN when using externally generated clock. This clock is supplied to each block of VRAM I/F, MPU I/F, and picture drawing processor.



VCKS (VCK signal select, input)
By selecting low level to VCKS, DCKIN input clock is used for the VRAM clock as well as the dot clock.

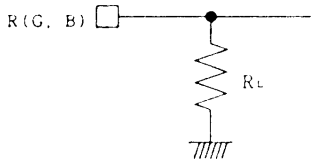
- **[Power Source]**

AVDD, AVSS (Analog power source, input)
Power supply to analog circuit. +5V for AVDD pin and ground level for AVSS pin

VDD, VSS (Digital power source, input)
Power supply to digital circuit. +5V for VDD pin and ground level for VSS pin

- **[Monitor Interface]**

R, G, B (Linear RGB, analog output)
Linear RGB signal output. With a 470Ω terminal resistance connected, 1Vp-p output voltage amplitude is output in 8-bit (256 levels) resolution.



/CSYNC (Composite SYNC signal (low active), output)
Composite SYNC signal output. Equivalent pulse is output in interlace mode.

/VSYNC (Vertical SYNC signal (low active), output)
Vertical SYNC signal output

/HSYNC (Horizontal SYNC signal (low active), output)
Horizontal SYNC signal output

DOTCK/AT (Dot clock/attribute bit, output)
2-dividing clock output of DCKIN pin input. RGB signal changes synchronously with this clock. Through internal register setting, AT bit is output instead of 2-dividing DCKIN clock.

FSC (Sub-carrier clock, output)
Sub-carrier clock output. Frequency is determined according to register setting.

/VRESET (Vertical timing reset (low active), input)
Synchronization with external display unit is possible by connecting /VSINC or /CSYNC of external display signal.

/HRESET (Horizontal timing reset (low active), input)
Horizontal timing of NVDP CRT controller block is reset.

YS (Superimposing timing, output)
Signal output to switch between NVDP RGB output and external video signal (when superimposing)

DCKIN, DCKOUT (XTAL input/output, input/output)
With XTAL connected, clock to generate display dot clock is oscillated.
(Refer to description of VCKIN, OUT and VCKS)

- **[Others]**

/TEST (Test, input)
Test. Always used in open(unconnected) condition.

■ FUNCTION DESCRIPTION

● Screen Mode

There are 5 screen modes as listed below.

- ◆ Three16-color screens + two sprite screens
- ◆ One 256-color screen + one 16-color screen + two sprite screens
- ◆ One16-color high resolution screen + one 16-color screen + two sprite screens
- ◆ One △YUV screen + one 16-color screen + two sprite screens
- ◆ One YUV 422 screen + two sprite screens

[Example of Screen Construction for Navigation System]

- ◇ 16-color A screen : Basic information such as roads and buildings.
- ◇ 16-color B screen : Additional information such as place names and signs.
- ◇ 16-color C screen : Application information such as menu, switch box and direction symbols.
- ◇ △YUV screen : Natural picture such as image service files
- ◇ YUV 422 screen : Motion picture by MPEG decoder
- ◇ Sprite A screen : Arrow cursor
- ◇ Sprite B screen : Vehicle marker

● Number of bits and number of colors for each picture element

◆ 16-color screen	4 bits/1 picture element	16 colors out of 260,000 colors
◆ 256-color screen	8 bits/1 picture element	256 colors out of 260,000 colors
◆ △YUV screen	8 bits/1 picture element	16,700,000 colors
◆ YUV screen	16 bits/1 picture element	16,700,000 colors
◆ Sprite screen	4 bits/1 picture element	16 colors out of 260,000 colors (*provided with built-in pattern RAM)

● VRAM Capacity and Image Space

The NVDP provides an image space for the number of dots obtained by dividing the capacity of the connected video memory by 4. (For example, when 1 unit of 4M DRAM is connected, a 1M dot image space is provided by 16-color screen conversion in all). The shape of the image space is selected by specifying the "X" size of 512, 1024, 2048, 4096, 8192 or 16384 dots. (However, the selectable sizes are limited depending on the connected DRAM.) The "Y" size is determined by the "X" size and the capacity of the DRAM being used.

		X Size					
VRAM	Total number of dots	512	1024	2048	4096	8192	16384
1 unit of 256K x 16	1024K	2048	1024	512	-	-	-
2 units of 512K x 8	2048K	4096	2048	1024	512	-	-
1 unit of 1M x 16	4096K	8192	4096	2048	1024	512	-
2 units of 245K x 16	2048K	4096	2048	1024	512	-	-
4 units of 512K x 8	4096K	8192	4096	2048	1024	512	-
2 units of 1M x 16	8192K	16384	8192	4096	2048	1024	512

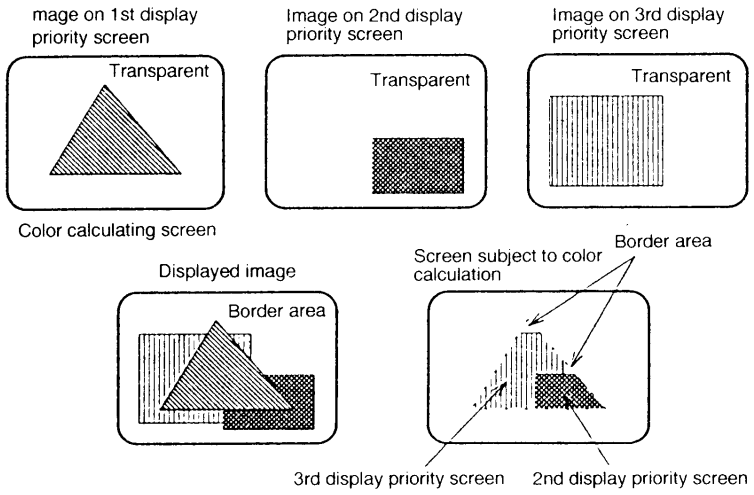
No setting is possible where marked with "-"

• Scrolling

The NVDP has 2 types of built-in scroll counters ("A", "B") both of which enable scrolling by dot unit. The scroll counter "A" is assigned to 1 unit of 16-color screen, 256-color screen and YUV screen and the scroll counter "B" to 1 unit of 16-color screen. For the remaining 1 unit of 16-color screen, either "A" scroll counter or "B" scroll counter can be selected. As scroll counters "A" and "B" can be set independently, functions such as scrolling the background map can be executed only by setting the display start register with the switch box display position fixed. Also, with the scroll counter "A", it is easy to realize the hardware head-up function to turn the area being displayed by 180°.

• Color Calculation

One screen (color calculating screen) is selected from among three 16-color screens, one 256-color screen and two sprite screens as a screen of the highest display priority. With images on other screens of lower display priority used simultaneously, color calculation is executed on these images and semitransparent display is available in 4 levels as described below. Whether to execute color calculation or not can be determined by the dot unit between the screen of the highest display priority and that of lower display priority.



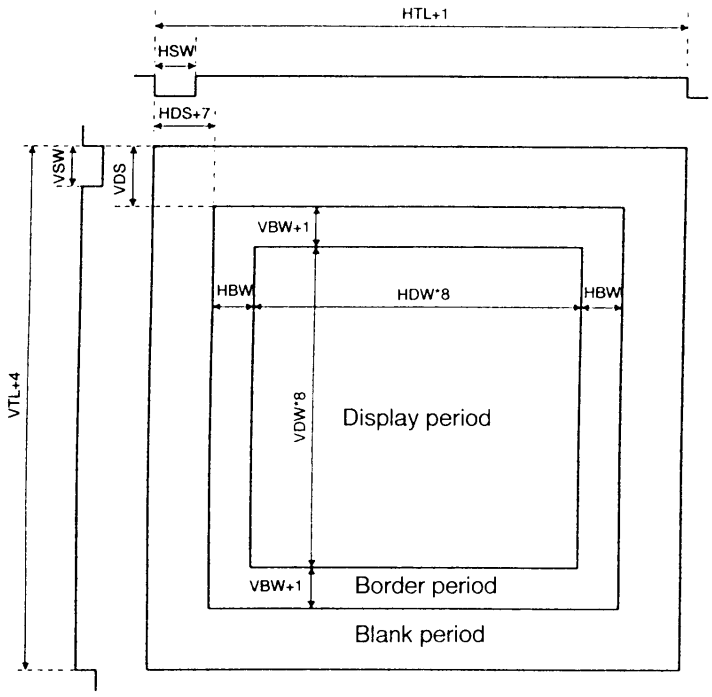
The values calculated by (Color calculating screen *I + screen subject to color calculation *J) become display colors for each of R, G, and B. For (I, J), one of (0/4, 4/4), (1/4, 3/4), (2/4, 2/4) and (3/4, 1/4) is selected. For the dot whose YSN signal is "0" or the dot of the non-color calculating screen, (4/4, 0/4) values are displayed for (I, J).

● Display Timing Control

The NVDP generates the display timing signal suitable for each monitor. The timing signal can be used for any desired display system such as home TV, various CRT monitors, LCD TV, LCD panel, etc. Display in the interlace mode is also available.

Display parameters that can be set are as follows.

Name	Symbol	Unit for setting
Horizontal cycle	HTL	10 bits by 1-dot unit (1024 dots max.)
Horizontal display dot number	HDW	6 bits by 8-dot unit (504 dots max.)
Horizontal display position	HDS	8 bits by 1-dot unit (256 dots max.)
Horizontal synchronous pulse width	HSW	6 bits by 1-dot unit (64 dots max.)
Horizontal border period	HBW	8 bits by 1-dot unit (256 dots max.)
Vertical cycle	VTL	9 bits by 1-line unit (512 lines max.)
Vertical display line number	VDW	6 bits by 8-line unit (504 lines max.)
Vertical display position	VDS	6 bits by 1-line unit (64 lines max.)
Vertical synchronous pulse width	VSW	3 bits by 1-line unit (8 lines max.)
Vertical border period	VBW	8 bits by 1-line unit (256 lines max.)



■ TYPICAL IMPLEMENTATION

Fig. 1-1 below shows an example of the application circuit using the NVDP. The NVDP connects directly to a 16-bit or 32-bit general-purpose microprocessor as a peripheral device.
The NVDP draws images into video memory in response to commands issued by the MPU, and outputs the image data of the video memory as a linear RGB signal (analog signal) in sync with monitor scan timing. The NVDP can connect to a maximum of 4MB of video memory (DRAM).
The NVDP includes a data arrangement function (for realignment of video-memory data into dot data) and a D/A converter. These internal features make it possible to construct a low-cost implementation using external DRAM and video encoder only.

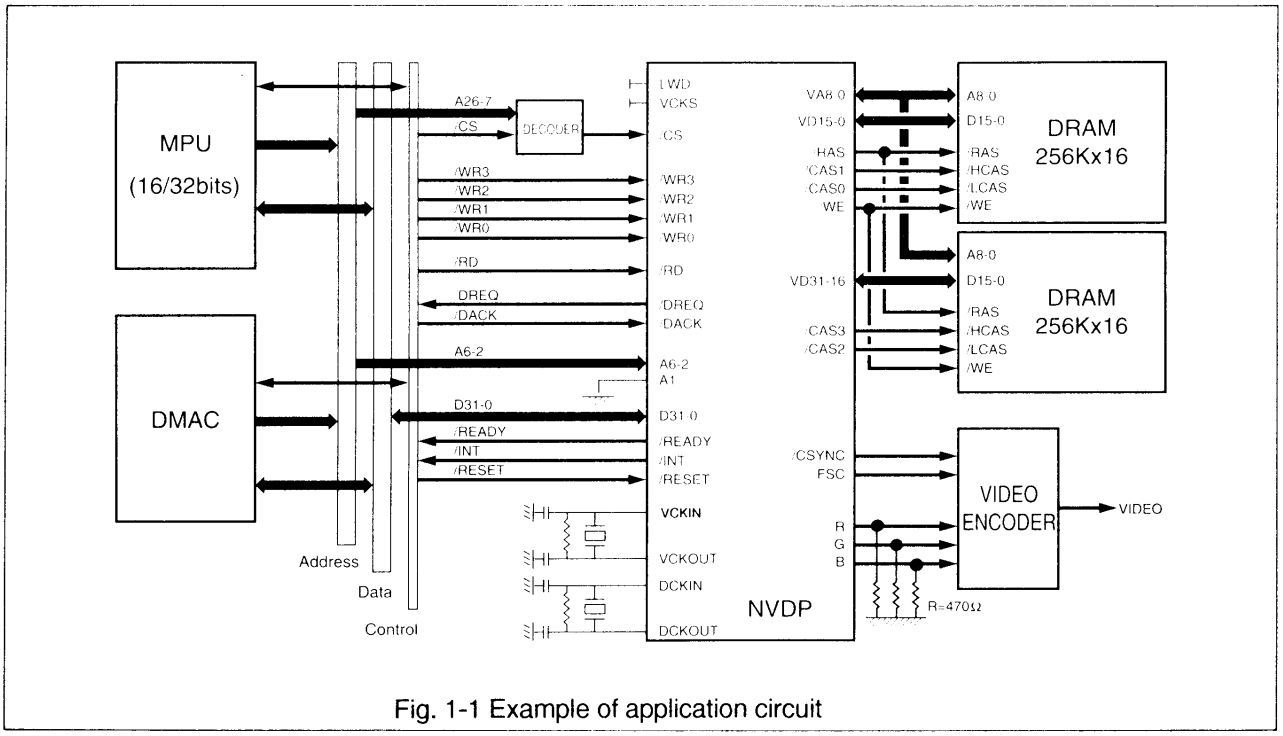
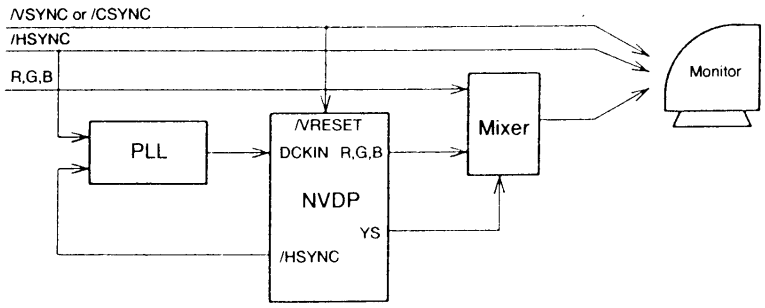


Fig. 1-1 Example of application circuit

- **Superimposing**

Inputting /CSYNC or /VSYNC of the external image signal into the /VRESET terminal enables to synchronize the vertical timing to the external image signal. When the external image signal and the /HSYNC signal output from the NVDP are locked by the PLL circuit and the display clock generated in the VCO circuit is supplied to the DCKIN terminal of the NVDP, the horizontal timing can be also synchronized to the external image signal. Superimposing is executed by using the YS signal output from the NVDP as the image select signal.



Example of system by external synchronization

■ ELECTRICAL CHARACTERISTICS

1.Absolute Maximum Rating

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}*1	-0.5～+7.0	V
Input terminal voltage	V_I*1	-0.5～V_{DD}+0.5	V
Output terminal voltage	V_O*1	-0.5～V_{DD}+0.5	V
Output terminal current	I_O	-20～+20	mA
Storage temperature	T_{stg}	-50～+125	℃

*1 Value with VSS(GND)=0V used as reference.

2.Recommended Operation Conditions

Item	Symbol	Min	Ref.	Max.	Unit
Power supply voltage	V_{DD}*1	4.75	5.00	5.25	V
Low level input voltage *2	V_{IL}*1	-0.3		0.8	V
High level input voltage *2	V_{IH}*1	2.0		V_{DD}+0.3	V
Low level input voltage *3	V_{IL}*1	-0.3		V_{DD}×0.3	V
High level input voltage *3	V_{IH}*1	V_{DD}×0.7		V_{DD}+0.3	mA
Operating ambient temperature	T_{OP}*4	-40		+85	℃

*1 Value with VSS(GND)=0V used as reference.

*2 DCKIN, VCKIN terminals excluded

*3 DCKIN, VCKIN terminals

*4 Inspection condition before shipment is 0～85°C

3.DC Characteristics

Item	Symbol	Min	Ref.	Max.	Unit
Low level output voltage	V_{OL}*1			0.4	V
High level output voltage *2	V_{OH}*3	4.0			V
Input leakage current	I_{LI}			10	μA*4
Output leakage current	I_{LO}			25	μA*4
Current consumption	I_{DD}		70		mA

*1 Measurement condition IOL = 1.6mA (Value with VSS(GND)=0V used as reference)

*2 Open Drain terminal excluded

*3 Measurement condition IOH = -1.0mA (Value with VSS(GND)=0V used as reference)

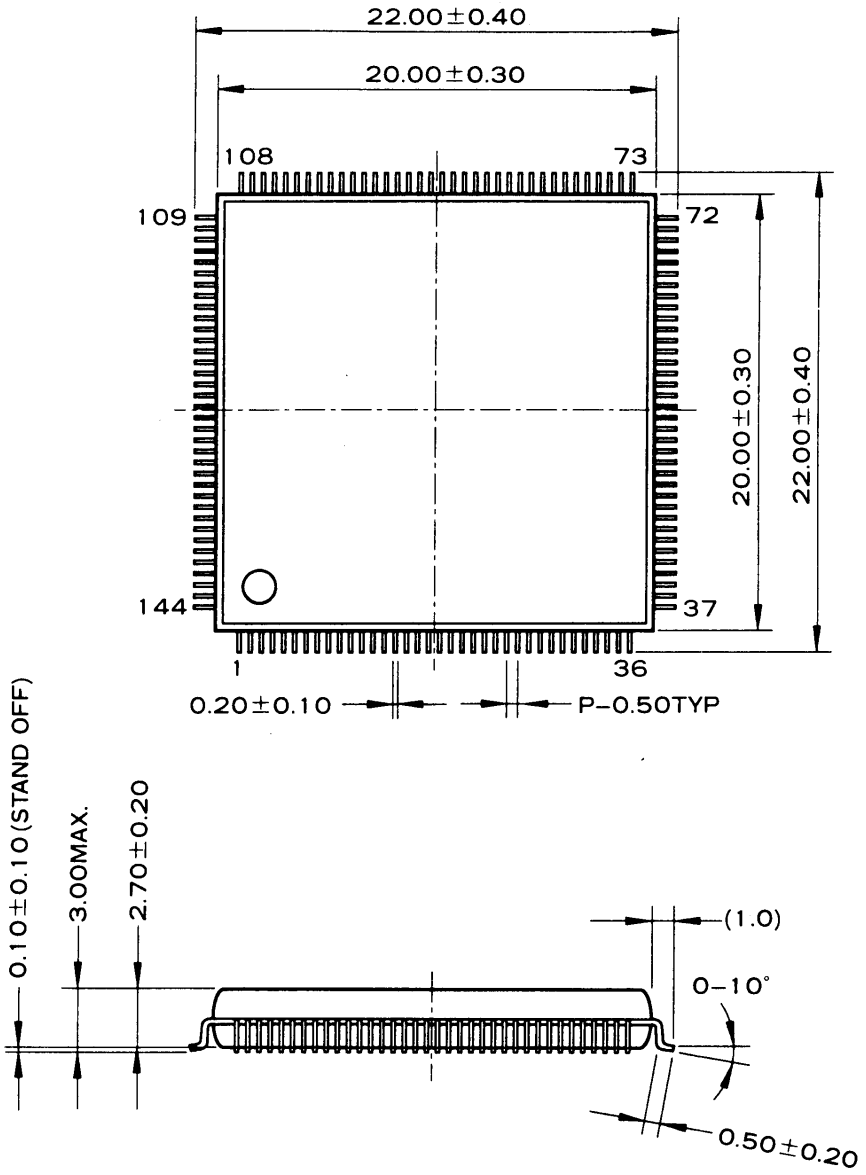
*4 uA: micro ampere (10-6A)

Electrical characteristics under recommended operation conditions

4.Terminal capacity

Item	Symbol	Min	Ref.	Max.	Unit
Input terminal capacity	C_I			8	F
Output terminal capacity	C_O			10	F
Input/output terminal capacity	C_{IO}			12	F

■ EXTERNAL DIMENSIONS



lead thickness : 0.125±0.05 or 0.15±0.05

DIMENSION IN mm

Note : The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

Note) Specifications of this product are subject to change for improvement without prior notice.

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