YAMAHA LSI

YMF752

Preliminary

AC'97 Rev2.1 Audio CODEC with SRC

■ OVERVIEW

YMF752 is an AC'97 Audio CODEC LSI, which is fully compliant with the industry standard "Audio CODEC '97" component specification (Revision 2.1).
YMF752 includes a SRC (Sampling Rate Converter) for supporting variable sampling rate and an AC-Link serial interface. Therefore, YMF752 is the best audio solution for both laptops and desktop PCs as well as AMR (Audio Modem Riser) and MDC (Mobile Daughter Card).
YMF752 also supports low power consumption while normal operating and allows for controlling the power down mode.

■ FEATURES

- AC'97 Revision 2.1 Compliant
- Exceeds PC98 / PC99 Audio Performance Requirements
- Analog Inputs:
  - 4 Stereo Inputs: LINE, CD, VIDEO, AUX
  - 2 Monaural Inputs: Speakerphone and PC BEEP Inputs
  - 2 Independent Microphone Inputs
- PC BEEP can directly output to Line Out
- Internal +20dB amplifier circuitry for microphone
- Analog Outputs: Stereo LINE Output, True LINE Level and Monaural Output
- Supports 3D Enhancement (Wide Stereo)
- Supports Variable Sampling Rate (48k/44.1k/22.05k/16k/11.025k/8kHz)
- Programmable Power Down Mode
- Supports EAPD (External Amplifier Power Down)
- Power Supplies: Analog 5.0V, Digital 3.3V
- 48-Pin SQFP Package (YMF752-S)

The following functions are supported by using the software driver from YAMAHA.

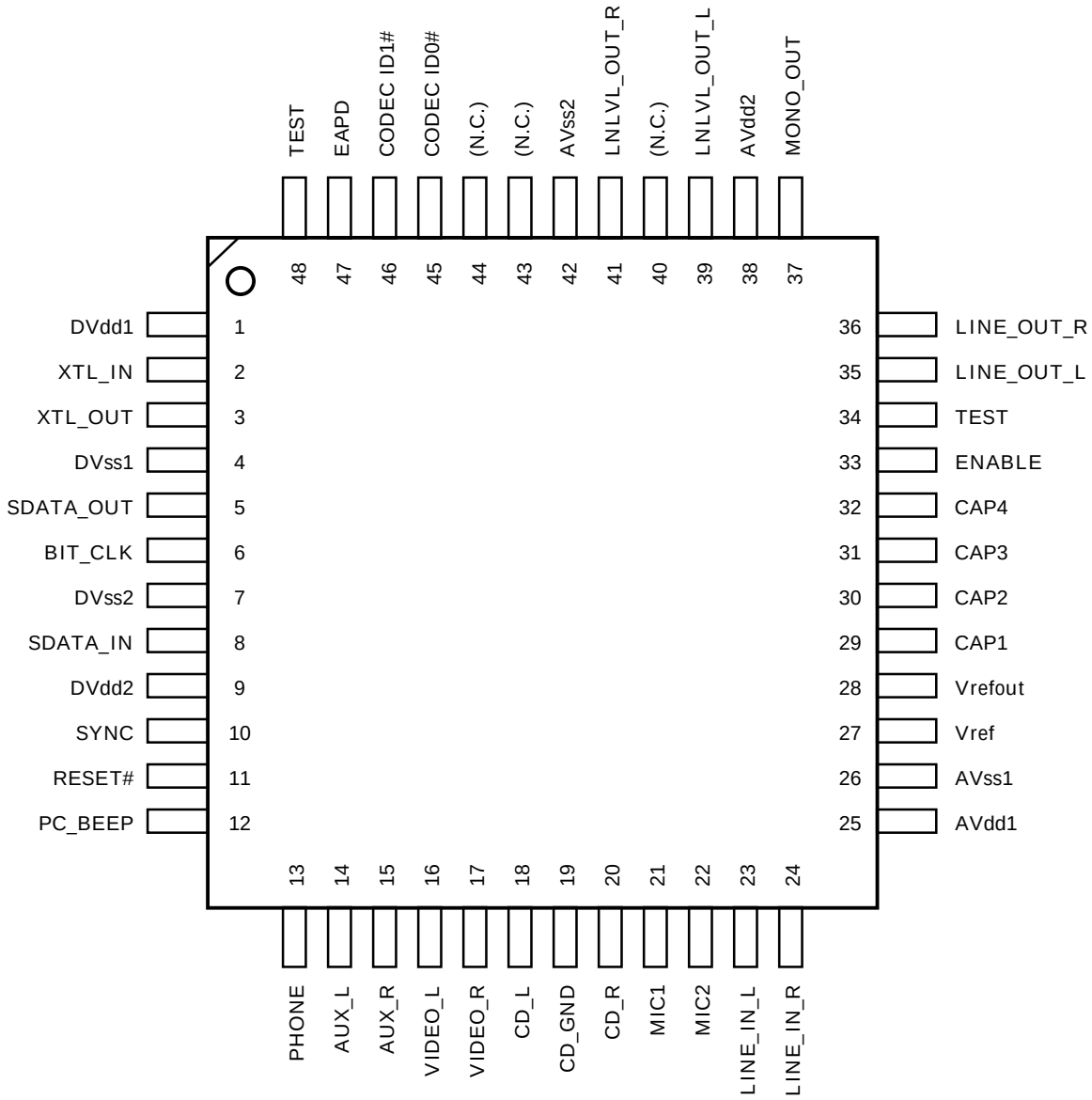
- XG Wave Table Synthesizer
- Downloadable Sound (DLS)
- Legacy Audio (Sound Blaster Pro compatibility and FM Synthesizer) on Pure DOS

The contents of this catalog are target specifications and are subject to change without prior notice. When using this device, please recheck the specifications.

YAMAHA CORPORATION

YMF752 CATALOG
CATALOG No.:LSI-4MF752A02
July 2, 1999

■ PIN CONFIGURATION



48-Pin SQFP Top View

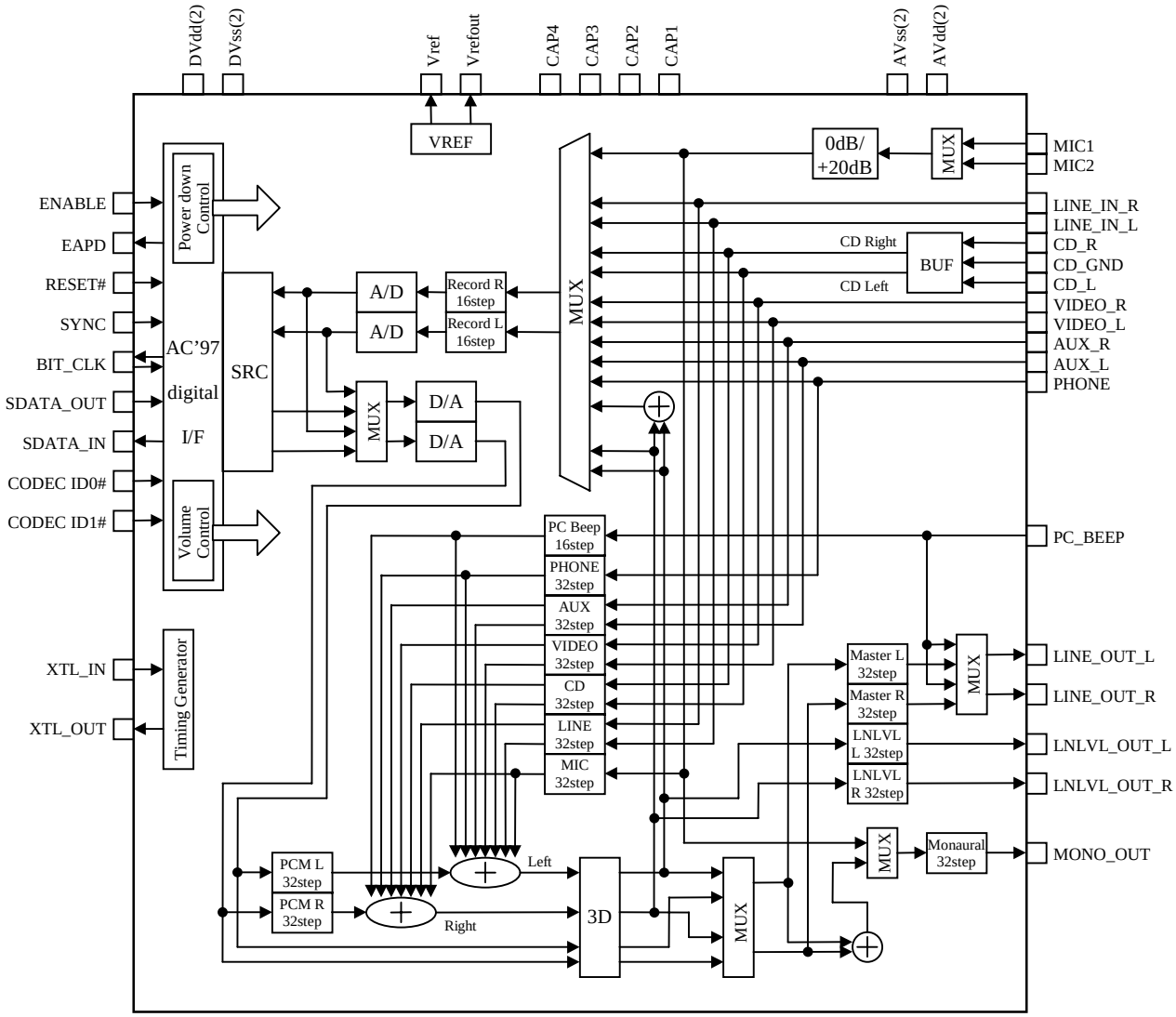
■ PIN DESCRIPTION

No.	Name	I/O	Function
1	DVdd1	-	Digital power supply (+3.3V) Connect to the digital ground with 0.1μF and 47μF capacitors. Connect this pin to DVdd2.
2	XTL_IN	I	24.576MHz Clock Input
3	XTL_OUT	O	24.576MHz Clock Output
4	DVss1	-	Digital ground. Connect this pin to DVss2.
5	SDATA_OUT	I	AC'97 Serial Input Stream
6	BIT_CLK	I/O	AC'97 Bit Clock
7	DVss2	-	Digital ground. Connect this pin to DVss1.
8	SDATA_IN	O	AC'97 Serial Output Stream
9	DVdd2	-	Digital power supply (+3.3V) Connect to the digital ground with 0.1μF and 47μF capacitors. Connect this pin to DVdd1.
10	SYNC	I	SYNC Input (Fixed at 48kHz)
11	RESET#	I	Hardware Reset
12	PC_BEEP	AI	PC Speaker Beep
13	PHONE	AI	Telephony Input
14	AUX_L	AI	AUX Input Left Channel
15	AUX_R	AI	AUX Input Right Channel
16	VIDEO_L	AI	Video Audio Input Left Channel
17	VIDEO_R	AI	Video Audio Input Right Channel
18	CD_L	AI	CD Audio Input Left Channel
19	CD_GND	AI	CD Audio Analog Ground Connect this pin to CD Ground or Analog Ground.
20	CD_R	AI	CD Audio Input Right Channel
21	MIC1	AI	Microphone Input 1
22	MIC2	AI	Microphone Input 2
23	LINE_IN_L	AI	Line Input Left Channel
24	LINE_IN_R	AI	Line Input Right Channel
25	AVdd1	-	Analog Power Supply (+5.0V) Connect to the analog ground with 0.1μF and 47μF capacitors. Connect this pin to AVdd2.
26	AVss1	-	Analog ground. Connect this pin to AVss2.
27	Vref	AO	Analog Reference Voltage Connect to the analog ground with 0.1μF and 10μF capacitors.
28	Vrefout	AO	Analog Reference Voltage Output

No.	Name	I/O	Function
29	CAP1	A	Capacitor Connection Pin Connect to the analog ground with a 560pF capacitor.
30	CAP2	A	Capacitor Connection Pin Connect to the analog ground with a 560pF capacitor.
31	CAP3	A	Capacitor Connection Pin Connect to the analog ground with a 1000pF capacitor.
32	CAP4	A	Capacitor Connection Pin Connect to the analog ground with 0.1μF and 10μF capacitors.
33	ENABLE	I+	Normally, do not connect externally. In case of “low” level, YMF752 do not operate.
34	TEST	I+	LSI Test Pin (Do not connect externally.)
35	LINE_OUT_L	AO	Line Output Left Channel
36	LINE_OUT_R	AO	Line Output Right Channel
37	MONO_OUT	AO	Monaural Output
38	AVdd2	-	Analog power supply (+5.0V) Connect to the digital ground with 0.1μF and 47μF capacitors. Connect this pin to Avdd1.
39	LNLVL_OUT_L	AO	True LINE Level Output Left Channel
40	(N.C.)	-	Do not connect externally.
41	LNLVL_OUT_R	AO	True LINE Level Output Right Channel
42	AVss2	-	Analog ground. Connect to Avss1.
43	(N.C.)	-	Do not connect externally.
44	(N.C.)	-	Do not connect externally.
45	CODEC ID0#	I+	CODEC ID (Do not connect externally.)
46	CODEC ID1#	I+	CODEC ID (Do not connect externally.)
47	EAPD	O	External Amplifier Power Down
48	TEST	O	LSI Test Pin (Do not connect externally.)

Note) AI: Analog Input Pin, AO: Analog Output Pin, I+: Input Pin with a Pull-up resistor

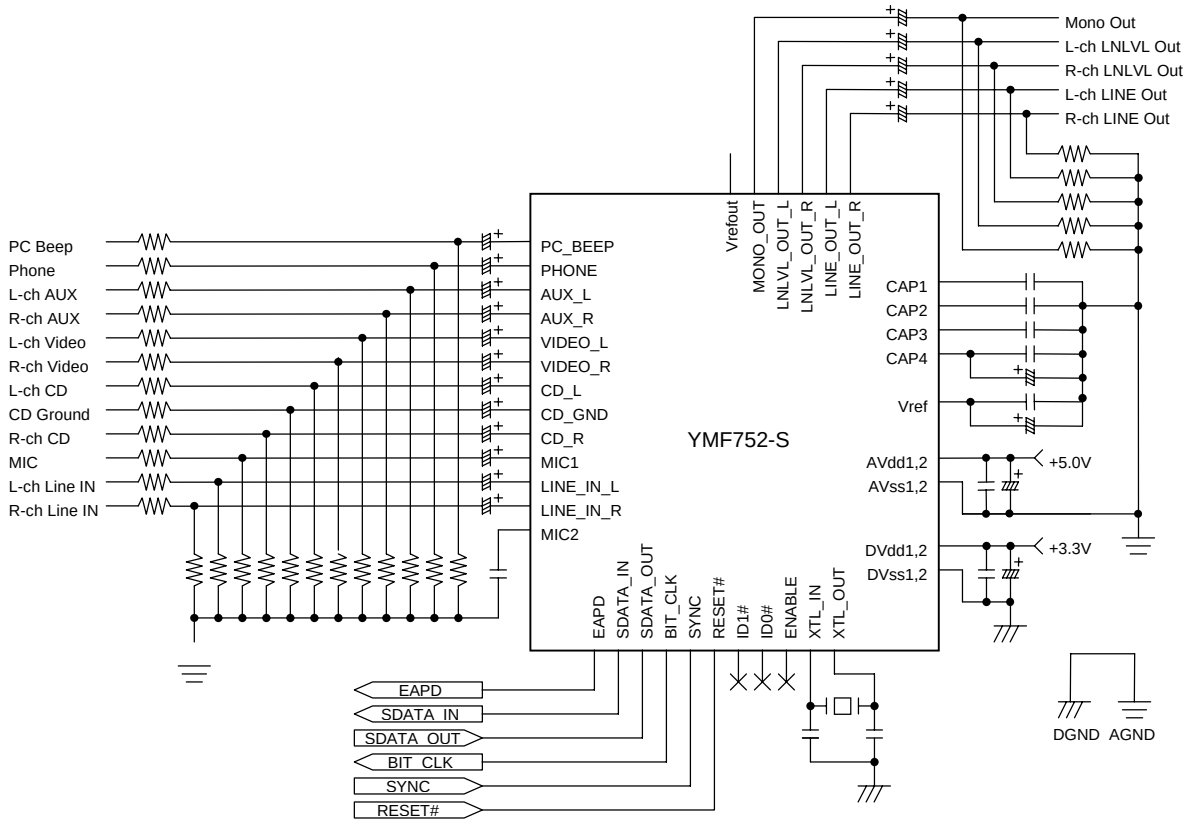
■ BLOCK DIAGRAM



■ MIXER REGISTERS

	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	Reset																
02h	Master vol.	Mute	-	ML5-0						-	-	MR5-0						8000h
04h	LNLVL vol.	Mute	-	ML5-0						-	-	MR5-0						8000h
06h	Master vol. Mono	Mute	-	-	-	-	-	-	-	-	-	MM5-0						8000h
0Ah	PC_BEEP vol.	Mute	-	-	-	-	-	-	-	-	-	-	PV3-0				-	0000h
0Ch	Phone vol.	Mute	-	-	-	-	-	-	-	-	-	-	GN4-0					8008h
0Eh	Mic vol.	Mute	-	-	-	-	-	-	-	-	20dB	-	GN4-0					8008h
10h	Line in vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
12h	CD vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
14h	Video vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
16h	Aux vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
18h	PCM out vol.	Mute	-	-	GL4-0					-	-	-	GR4-0					8808h
1Ah	Record Select	-	-	-	-	-	SL2-0			-	-	-	-	-	SR2-0			0000h
1Ch	Record Gain	Mute	-	-	-	GL3-0				-	-	-	-	GR3-0				8000h
20h	General Purpose	POP	-	3D	-	-	-	MIX	MS	LPBK	-	-	-	-	-	-	-	0000h
22h	3D Control	-	-	-	-	-	-	-	-	-	-	-	-	DP3-0				0000h
26h	Power Down	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	-	-	-	-	REF	ANL	DAC	ADC	N/A
28h	Extended Audio ID	ID1	ID0	-	-	-	-	AMAP	-	-	-	-	-	-	-	-	VRA	x201h
2Ah	Ext'd audio Stat/Ctrl	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	VRA	0000h
2Ch	PCM DAC Rate	SR15-0																BB80h
32h	PCM ADC Rate	SR15-0																BB80h
7Ch	Vendor ID 1	Vendor ID																
7Eh	Vendor ID 2																	

■ SYSTEM CONNECTION DIAGRAM



1) Power and Ground

To get the most out of analog performance, it is necessary to split the ground into analog and digital blocks. Analog ground and digital ground earth at one point closed to the initial ground supply of the board. The layout of the ground pattern should be designed as large as possible and the impudence should be reduced to prevent from receiving ambient noise. In addition, use 0.1μF and 47μF capacitors to connect between the analog voltage pin and the analog ground as well as between the digital supply pin and the digital ground.

2) Reference Voltage

As the reference voltage determines all analog signals' reference levels of YMF752, noise generated from the reference voltage could affect the YMF752's analog performance. To stabilize the YMF752's reference voltage, insert a 0.1μF ceramic capacitor in parallel with a 10μF capacitor between Vref pin and the ground. The 0.1μF ceramic capacitor should be designed as close to the Vref pin as possible

3) Master Clock

To suppress the master clock from affecting its surroundings, it is recommended to keep the master clock guarded on the ground so the noise can be reduced.

4) Unused Analog Input / Output pins

For the unused analog input pins, short them through a 0.1μF ceramic capacitor to the analog ground. For the unused analog output pins, they should be left opened.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Analog Supply Voltage	AV_{DD}	-0.3	7.0	V
Digital Supply Voltage	DV_{DD}	-0.3	4.6	V
Analog Input Voltage	V_{INA}	-0.3	AV_{DD}+0.3	V
Digital Input Voltage	V_{IND}	-0.3	DV_{DD}+0.3	V
Ambient Temperature	T_{OP}	0	70	°C
Storage Temperature	T_{STG}	-50	125	°C

Note) $DV_{SS} = AV_{SS} = 0V$

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Analog Operating Voltage	AV_{DD}	4.75	5.00	5.25	V
Digital Operating Voltage	DV_{DD}	3.135	3.30	3.465	V
Operating Ambient Temperature	T_{OP}	0	25	70	°C

Note) $DV_{SS} = AV_{SS} = 0V$

3. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level 1 Input Voltage	V_{IH1}	*1	$0.7 \times DV_{DD}$	-	-	V
Low Level 1 Input Voltage	V_{IL1}	*1	-	-	$0.3 \times DV_{DD}$	V
High Level 2 Input Voltage	V_{IH2}	*2	$0.8 \times DV_{DD}$	-	-	V
Low Level 2 Input Voltage	V_{IL2}	*2	-	-	$0.2 \times DV_{DD}$	V
High Level Output Voltage	V_{OH}	I_{OUT} = -1mA	DV_{DD} - 0.55	-	-	V
Low Level Output Voltage	V_{OL}	I_{OUT} = 1mA	-	-	0.55	V
Input Leakage Current	I_{LI}		-10	-	10	µA
Pull-up Resistance	R_{UP}		50	100	200	kΩ

Note) T_{OP}=0~70°C, DV_{DD}=3.3±0.165V, AV_{DD}=5.0±0.25V, Capacitor load=50pF

*1 : Apply to XTL_IN, RESET#, SYNC, SDATA_OUT and BIT_CLK

*2 : Apply to CODEC ID0# and CODEC ID1#

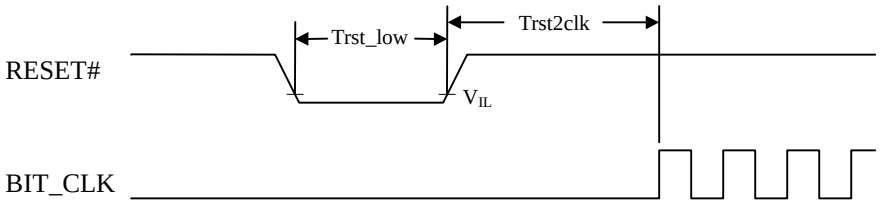
4. AC Characteristics

4-1. Reset

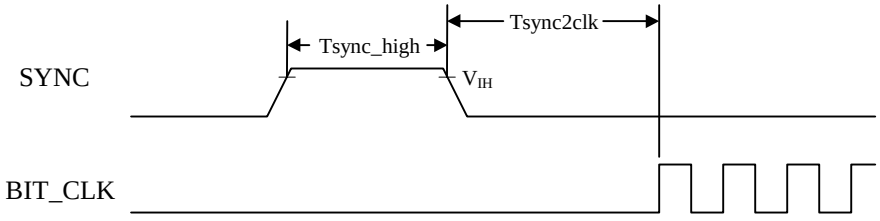
Parameter	Symbol	Min.	Typ.	Max.	Unit
Cold Reset (SDATA_OUT="L", SYNC="L")					
RESET# active low pulse width	Trst_low	1.0	-	-	µs
RESET# inactive to BIT_CLK start up delay	Trst2clk	162.8	-	-	ns
Warm Reset					
SYNC active high pulse width	Tsync_high	1.0	1.3	-	µs
SYNC inactive to BIT_CLK start up delay	Tsync2clk	162.8	-	-	ns

Note) T_{OP}=25°C, AV_{DD}=5.0V, Capacitor load=50pF

Cold Reset



Warm Reset

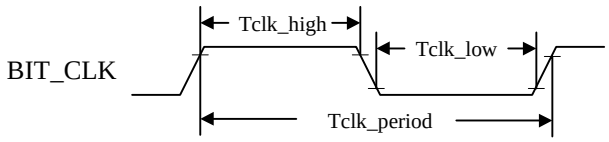


4-2. AC-link Interface

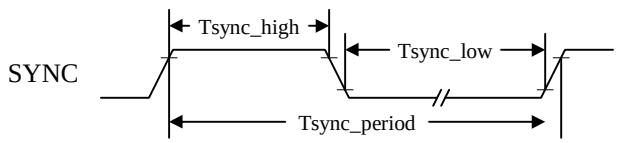
Parameter	Symbol	Min.	Typ.	Max.	Unit
BIT_CLK clock period	Tclk_period	-	81.38	-	ns
BIT_CLK low pulse width	Tclk_low	36.0	40.7	45.0	ns
BIT_CLK high pulse width	Tclk_high	36.0	40.7	45.0	ns
BIT_CLK rise time	Trise_clk	-	-	6	ns
BIT_CLK fall time	Tfall_clk	-	-	6	ns
SYNC period	Tsync_period	-	20.8	-	µs
SYNC low pulse width	Tsync_low	-	19.5	-	µs
SYNC high pulse width	Tsync_high	-	1.3	-	µs
SYNC rise time	Trise_sync	-	-	6	ns
SYNC fall time	Tfall_sync	-	-	6	ns
SDATA_IN, SDATA_OUT setup time	Tsetup	10.0	-	-	ns
SDATA_IN, SDATA_OUT hold time	Thold	10.0	-	-	ns
SDATA_IN delay time	Tdelay	-	-	15.0	ns
SDATA_IN rise time	Trise_din	-	-	6	ns
SDATA_IN fall time	Tfall_din	-	-	6	ns
SDATA_OUT rise time	Trise_dout	-	-	6	ns
SDATA_OUT fall time	Tfall_dout	-	-	6	ns
AC-link Low Power Mode End of slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdwn	-	-	1.0	µs
Active Test Mode					
Setup to trailing edge of RESET#	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z	Toff	-	-	50	ns

Note) T_{OP}=25°C, AV_{DD}=5.0V, Capacitor load=50pF

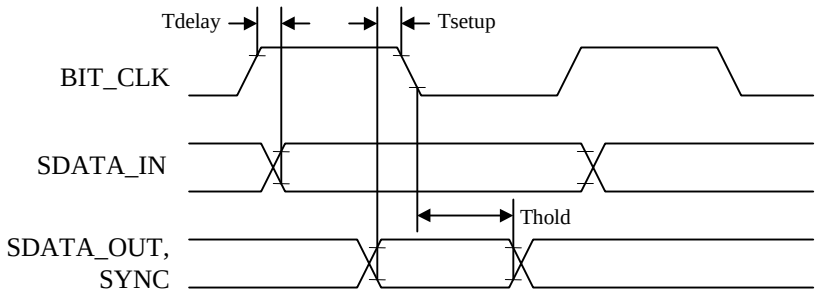
BIT_CLK



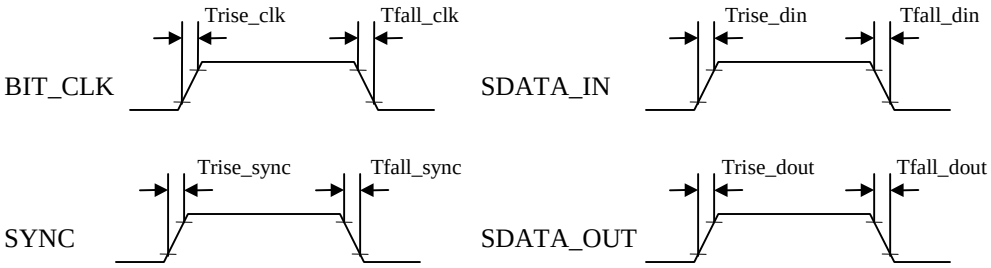
SYNC



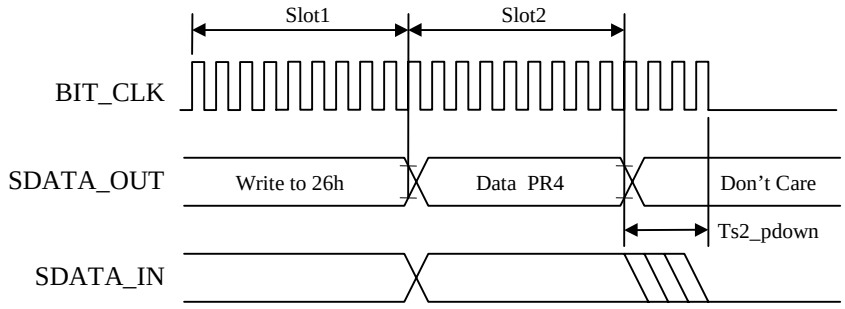
Setup and Hold



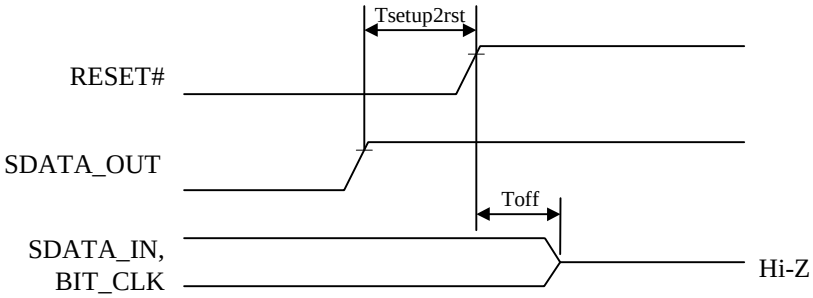
Signal Rise and Fall



AC-link Low Power Mode



Activate Test Mode



5. Power Consumption

Parameter	Min.	Typ.	Max.	Unit
Normal Operating (26h : PR6-0 = "0")				
AV_{DD}				mA
DV_{DD}				mA
Power Down Mode (26h : PR6-0 = "1")				
AV_{DD}				mA
DV_{DD}				mA

Note) T_{OP}=25°C, DV_{DD}=3.3±0.165V, AV_{DD}=5.0±0.25V

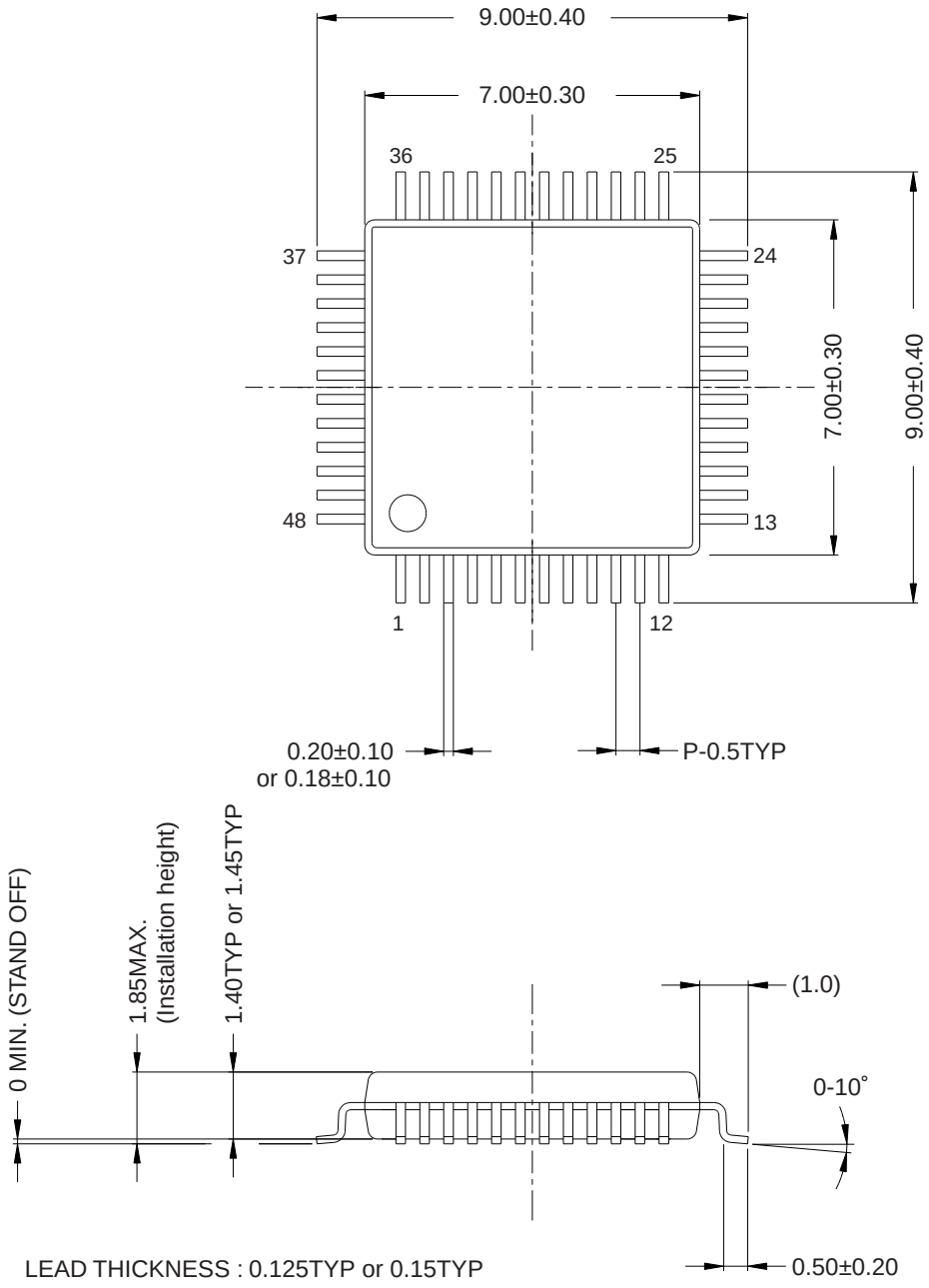
6. Analog Characteristics

Parameter	Min.	Typ.	Max.	Unit
Full Scale Line Input		1.0		Vrms
Full Scale Microphone Input (0dB)		1.0		Vrms
Full Scale Microphone Input (+20dB)		0.1		Vrms
Full Scale Line Output		1.0		Vrms
Analog S/N : CD to LINE_OUT	90	102		dB
Analog S/N : Others to LINE_OUT		102		dB
Analog Frequency Response	20		20,000	Hz
S/N : D/A converter	85	96		dB
S/N : A/D converter	75	86		dB
THD : Line Output			0.02	%
D/A & A/D Frequency Response	20		19,200	Hz
Transition Band	19,200		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	85			dB
Out-of-Band Rejection		40		dB
Group Delay			1	ms
Power Supply Rejection Rate (1kHz)		40		dB
Crosstalk between Inputs Channels			-70	dB
Attenuation & Gain Step				
PC_BEEP		3.0		dB
Other than PC_BEEP		1.5		dB
Input Impedance	10			kΩ
VREF Output Voltage		2.5		V

Note) T_{OP}=25°C, DV_{DD}=3.3±0.165V, AV_{DD}=5.0±0.25V, 1kHz input sine wave

■ EXTERNAL DIMENSIONS

YMF752-S



The actual shape of the molded corner may slightly differ from the shape in this diagram.
The figures in the parenthesis ( ) should be used as reference values.
The dimensions of plastic body do not include burr of resin.
Unit : mm (millimeters)
Note : The LSIs for surface mounting need for special care on storage and soldering conditions.
For detailed information, please contact your nearest agent of Yamaha.

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