YAMAHA LSI

YSF224B

Sound Analysis Processor (SAP)

■ OUTLINE

YSF224B (SAP) is a digital processing LSI which performs frequency filtering and level detection necessary for spectrum analysis of the audio signals.
The level data is output to the microprocessor in the decibel value through the serial interface.

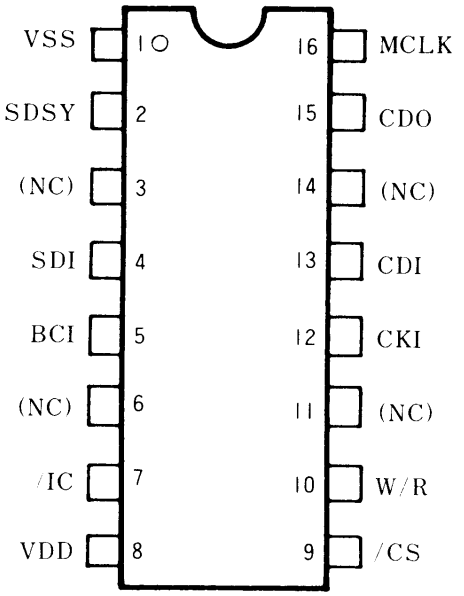
■ FEATURES

- Level detection processing is performed on the digital data of 32k to 48kHz sampling frequency.
- De-emphasis compensation is performed before the level is detected.
- Using the 2nd order IIR filter, the level detection of the bands up to seven bands and the total level detection are possible.
- The band frequency can be also set arbitrarily.
- The time constant of the peak holding for level detection can be also set arbitrarily.
- The level data is output in the decibel value of 3-dB resolution.
- Control is done by the microprocessor with a serial interface.
- The master clock is selected from 384fs or 256fs.
- 5V single power supply and Si-gate CMOS process.
- 16 pin plastic DIP (YSF224B-D) or 16 pin plastic SOP (YSF224B-M)

YAMAHA CORPORATION

YSF224B CATALOG
CATALOG No. : LSI-4SF2244
1994.04

■ PIN CONFIGURATION



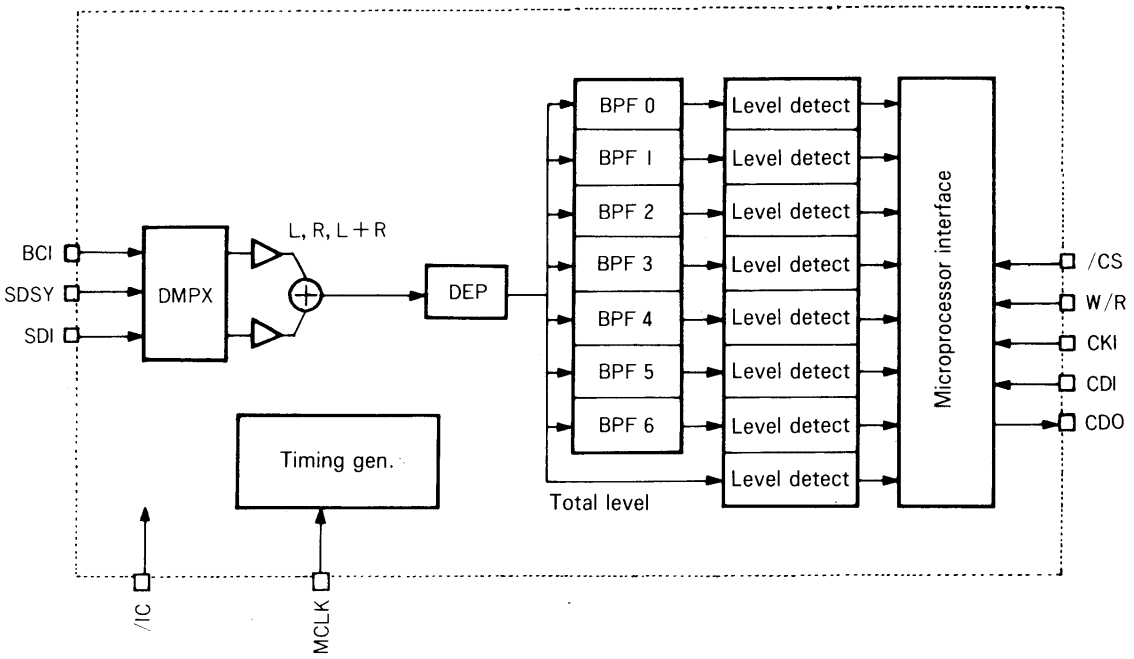
< Top View, common to 16DIP and 16SOP >

■ PIN FUNCTION

No.	Name	I/O	Function
1	VSS	—	Ground
2	SDSY	I	Digital audio signal input Word clock
3	(NC)		
4	SDI	I	Digital audio signal input Serial data
5	BCI	I	Digital audio signal input Bit clock
6	(NC)		
7	/IC	I+	Initial clear input
8	VDD	—	5V power supply
9	/CS	I	Microprocessor interface Chip select
10	W/R	I	Microprocessor interface Read/write control
11	(NC)		
12	CKI	I	Microprocessor interface Serial clock
13	CDI	I	Microprocessor interface Serial data input
14	(NC)		
15	CDO	O	Microprocessor interface Serial data output
16	MCLK	I	Master clock input (384fs or 256fs)

(NOTE) I+ : Input terminal with a pull-up resistor

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

1. Clock MCLK

An external clock of 384fs or 256fs is input through MCLK terminal.

2. Digital audio signal input BCI, SDSY, SDI

Digital audio siganls are input through BCI, SDSY and SDI terminals.

It is possible to obtain MSB-side 16 bit data from 16/18/20/24 bit data and setting is done through the microprocessor interface.

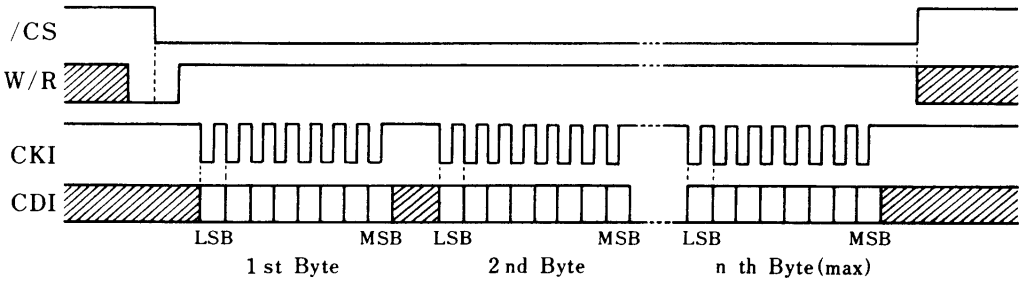
BCI, SDSY and SDI terminals must be synchronized with MCLK clock.

Also, BCI terminal must be one of 32fs, 48fs, 64fs, 96fs, 128fs and 192fs when MCLK terminal is 384fs and one of 32fs, 64fs and 128fs when MCLK is 256fs.

3. **Microprocessor interface /CS, W/R, CKI, CDI, CDO**

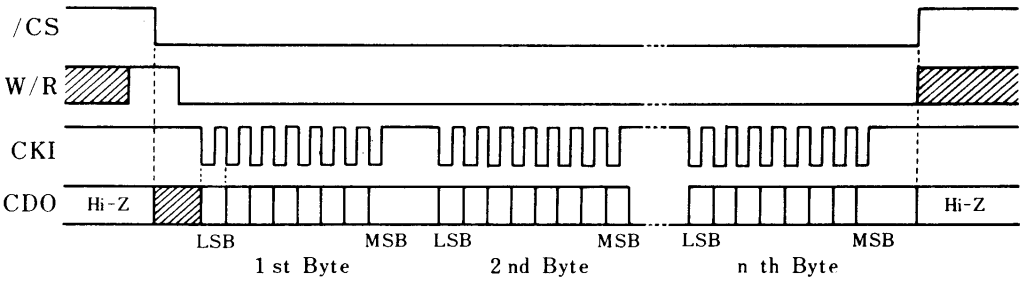
The first step is to set the operation mode by using each command.
After that, each level data can be read steadily in the set mode.

• Command write timing



NOTE : The shaded section means "don't care".

• Data read timing



NOTE : The shaded section means "don't care".
CDO terminal becomes high impedance when /CS terminal is at "H".

NOTE) To control a multiple number of this LSI with the same microprocessor, a period during which all /CS terminals become 'H' should be obtained for a period longer than 1 clock at 128fs when switching /CS terminal so that contention of CDO terminals is avoided.

4. **Initial clear /IC**

This LSI requires an initial clear when the power is turned on.

■ CONTROLS

1. Command

The command is largely classified by the upper 2 bits.

(a) Operation setting command (1 byte)

MSB	b6	b5	b4	b3	b2	b1	LSB
0	0	R	L	FS1	FS0	2/3	EN1

Bit 1 and 0 are reset to '0' at initial clear.

R, L : Mixing selection

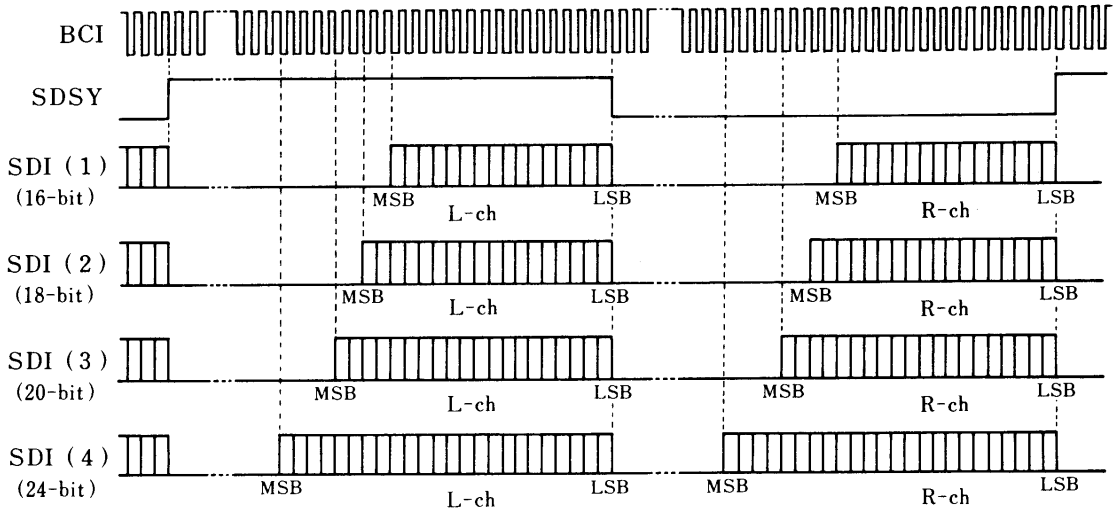
The signal for level detect processing is selected.

b5	b4	Audio signal to be processed
R	L	
0	0	Prohibited
0	1	L only
1	0	R only
1	1	L+R

FS1, FS0 : Input data format selection

b3	b2	Input format
FS1	FS0	
0	0	SDI (1)
0	1	SDI (2)
1	0	SDI (3)
1	1	SDI (4)

(NOTE) The data processed internally is always fixed to 16 bits from MSB.



2/3 : Master clock selection

0=384fs

1=256fs

EN1 : Signal process enable

0=Internal temporary RAM clear

1=Normal signal processing

(b) Output data setting command (1 byte)

MSB	b6	b5	b4	b3	b2	b1	LSB
0	1	TEST	LRS	OM	D2	D1	D0

TEST : LSI test

Be sure to set to '0'.

LRS : Level data reset

Reset the level data at '1', and the level data output mode will be retained.

OM : Level data output mode setting

0=The level data of the fixed channel is output (The channel is set by D2, D1 or D0).

1=The level data of each channel is output one after another (The initial channel is set by D2, D1 or D0).

D2, D1, D0 : Channel setting

CHANNEL=D2*4+D1*2+D0 (0 to 6 correspond to BPF0 to BPF6 while 7 to the total level.)

(c) Time constant setting command for level detection (1 byte)

MSB	b6	b5	b4	b3	b2	b1	LSB
1	0	TEST	D4	D3	D2	D1	D0

TEST : LSI test

Be sure to set to '0'.

D4 to D0 : Time constant setting

Set the peak hold time constant (time required for −6dB attenuation) for level detection.

(Peak hold time constant)=(D4 × 16+D3 × 8+D2 × 4+D1 × 2+D0+1) × 1024 × (sampling cycle time)

However, peak hold time constant becomes ∞ when D4=D3=D2=D1=D0=0.

(d) Coefficient write command (n byte)

MSB	b6	b5	b4	b3	b2	b1	LSB	1st Byte
1	1	EN0	R4	R3	R2	R1	R0	

MSB	b6	b5	b4	b3	b2	b1	LSB	2nd Byte
D1	D0	*	*	*	*	*	*	

MSB	b6	b5	b4	b3	b2	b1	LSB	3rd Byte
D9	D8	D7	D6	D5	D4	D3	D2	

MSB	b6	b5	b4	b3	b2	b1	LSB	4th Byte
D17	D16	D15	D14	D13	D12	D11	D10	

(NOTE) * : don't care

EN0 : Signal process enable

Be sure to set to '1'.

R4 to R0 : Coefficient address

Set the coefficient address by using the lower 5 bits of the first byte, and the following 3-byte data are written as coefficient values. After that, only the coefficient values can be sent to the continuous addresses.

The internal band filter consists of the second order IIR filter and has 7 channels from BPF0 to 6. For each filter, it is necessary to set 3 coefficients, A, B and C.

The filter for de-emphasis consists of the first order IIR filter. Also, it is necessary to set 3 coefficients, D, E and F.

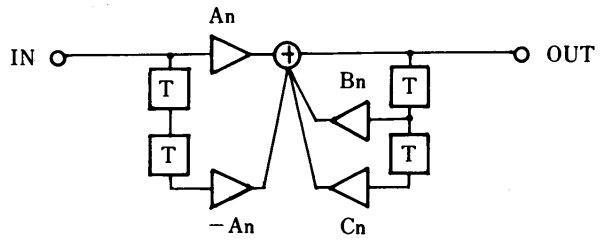
These coefficient addresses are determined as shown below.

COEF. ADDR		R4	0	0	0	0	1	1	1	1
		R3	0	0	1	1	0	0	1	1
		R2	0	1	0	1	0	1	0	1
R1	R0	HEX	0	4	8	C	10	14	18	1C
0	0	+0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	D
0	1	+1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	E
1	0	+2	C_0	C_1	C_2	C_3	C_4	C_5	C_6	F

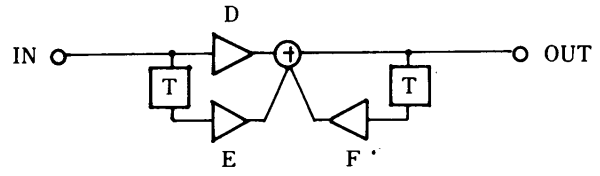
CHANNEL=R4*4+R3*2+R2
(0 to 6 correspond to BPF0 to BPF6 while 7 to DEP.)

(NOTE) When the data is written continuously, if the lower 2 bits of the address R1 and R0 are '1', it is skipped for further increment.

〈BPF0～6〉



〈DEP〉



D17 to D0 : Coefficient values

The coefficient value is 18 bits and 2's complement.

$$\text{(Coefficient value)} = \left\{ (-1) \times D_{17} + \sum_{n=0}^{16} Dn \times 2^{n-17} \right\} \times 2$$

2. Output data

MSB	b6	b5	b4	b3	b2	b1	LSB
0	0	0	L4	L3	L2	L1	L0

The level data is output in the decibel value of 3-dB resolution.

(Level data)=(−48)*L4+(−24)*L3+(−12)*L2+(−6)*L1+(−3)*L0 [dB]

The output channel and the order are determined by the output data setting commands.

■ ELECTRIC CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.3	V
Operating temperature	T_{op}	−40 ~ 85	°C
Storage temperature	T_{stg}	−50 ~ 125	°C

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	5.0	5.5	V
Operating temperature	T_{op}	0	25	70	°C

3. DC characteristics

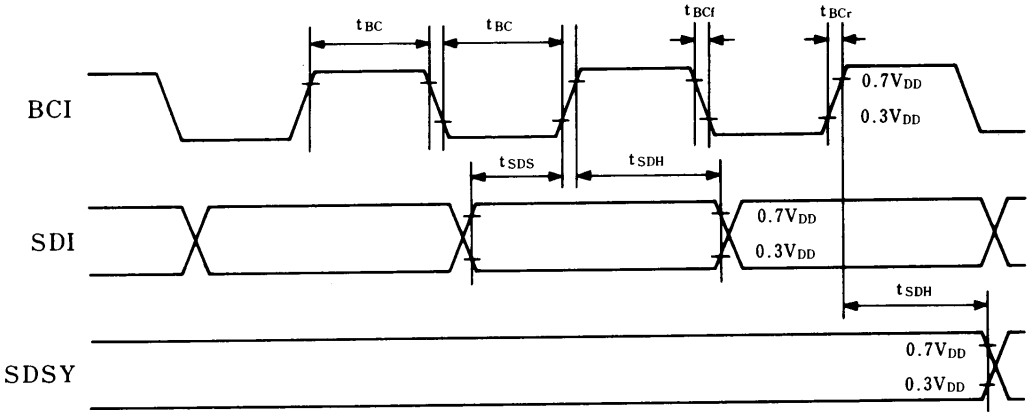
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{DD}	V_{DD}=5.5V			10	mA
Input voltage L level	V_{IL}				0.3V_{DD}	V
Input voltage H level	V_{IH}		0.7V_{DD}			V
Input leakage current	I_{LI}	*1	−1		1	μA
Output voltage L level	V_{OL}	I_{OL}=0.5mA, *2			0.4	V
Output voltage H level	V_{OH}	I_{OH}=−0.2mA, *2	V_{DD}−0.5			V
Output leakage current	I_{LO}	CDO terminal	−10		10	μA
Pull-up resistance	R_U	/IC terminal	60		600	kΩ
Input capacitance	C_I	f=1 MHz			8	pF
Output capacitance	C_O	f=1 MHz			10	pF

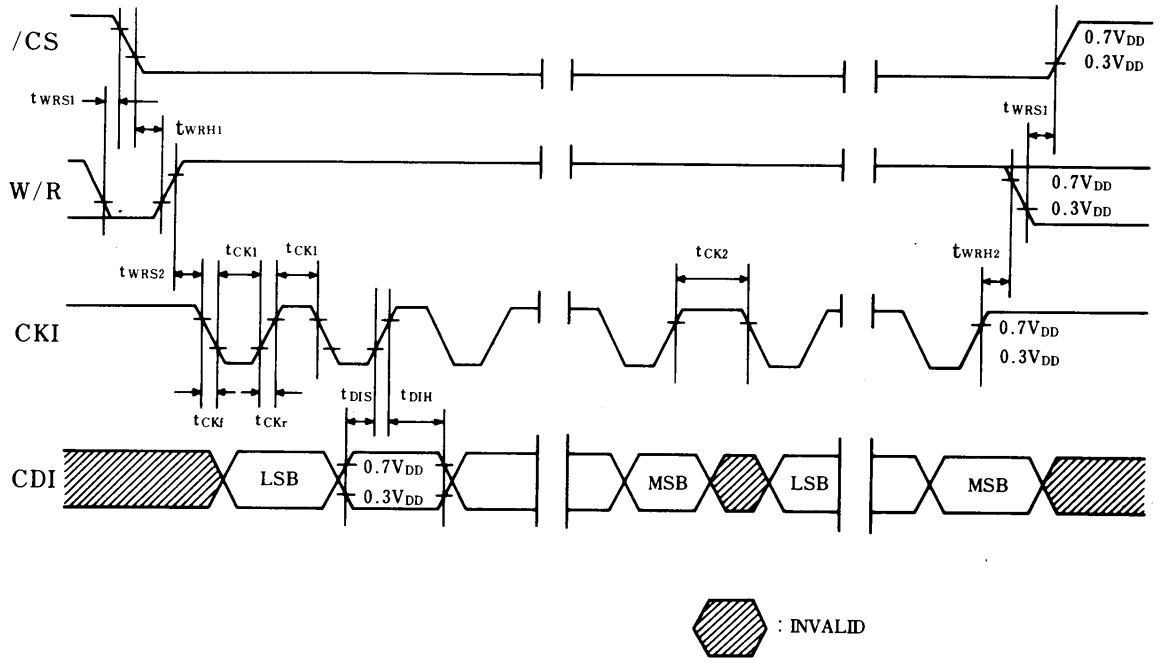
*1) Applicable to CKI, CDI, W/R, /CS, BCI, SDI, SDSY and MCLK terminals.
*2) Applicable to CDO terminal.

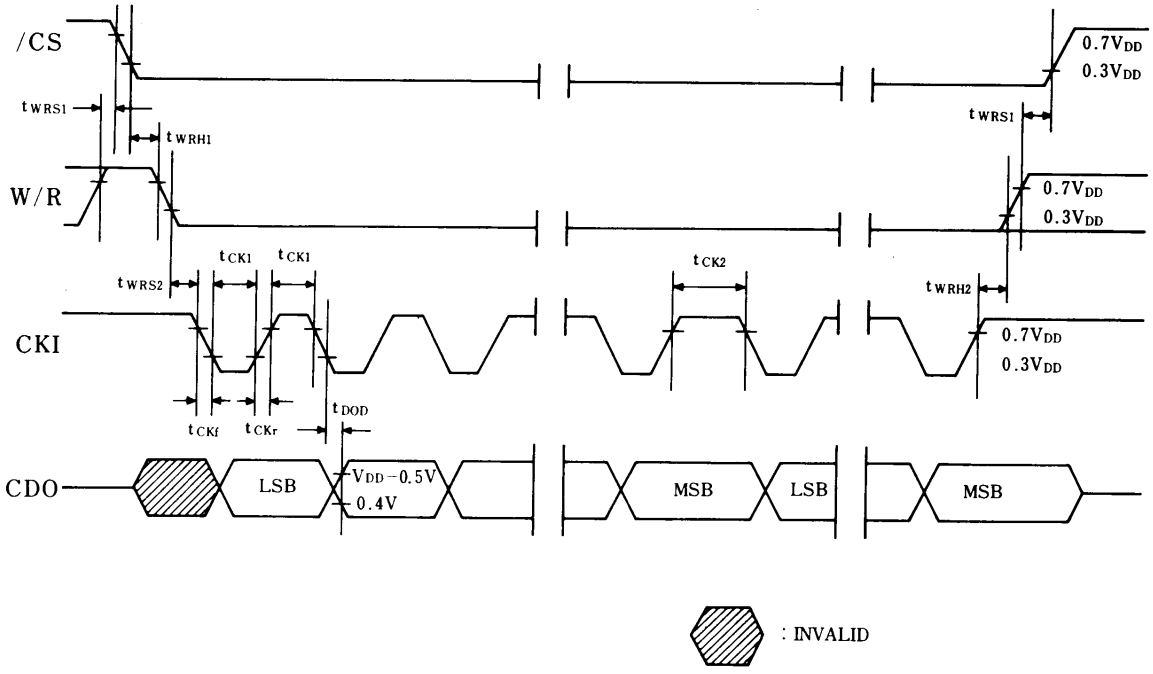
4. AC Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit
MCLK	frequency	f_{MC}	8.1		18.5	MHz
	duty	D_{MC}	40	50	60	%
BCI	ON·OFF time	t_{BC}	50			ns
	rise time	t_{BCr}			50	ns
	fall time	t_{BCf}			50	ns
SDI	setup time	t_{SDS}	20			ns
SDI, SDSY	hold time	t_{SDH}	20			ns
CDI	setup time	t_{DIS}	20			ns
	hold time	t_{DIH}	20			ns
CKI	ON·OFF time	t_{CK1}	100			ns
	ON time	t_{CK2}	5tc			s
CKI	rise time	t_{CKr}			50	ns
	fall time	t_{CKf}			50	ns
CDO	delay time	t_{DOD}			120	ns
W/R	setup time (1)	t_{WRS1}	tc			s
	hold time (1)	t_{WRH1}	tc			s
	setup time (2)	t_{WRS2}	4tc			s
	hold time (2)	t_{WRH2}	3tc			s

*1) tc=1/128fs

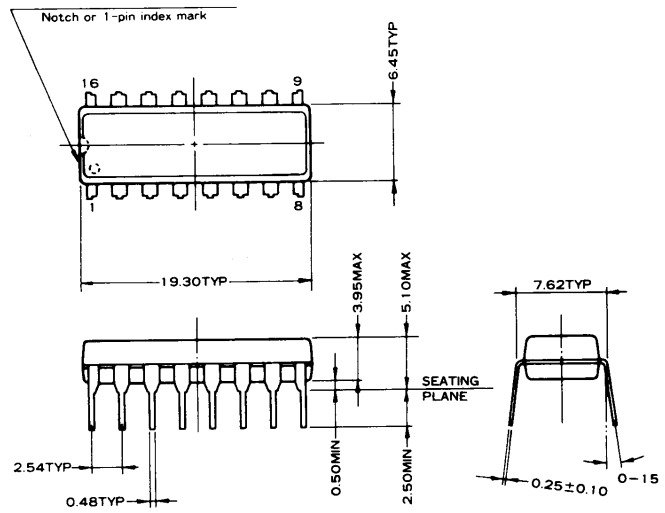



/CS
W/R
CKI
CDI
tWRS1
tWRH1
tWRS2
tCK1
tCK1
tCK2
tWRH2
tCKf
tCKr
tDIS
tDIH
0.7VDD
0.3VDD
LSB
MSB
LSB
MSB
: INVALID


/CS
W/R
CKI
CDO
tWRS1
tWRH1
tWRS2
tCK1
tCK1
tCK2
tWRH2
tCKf
tCKr
tDOD
0.7VDD
0.3VDD
VDD−0.5V
0.4V
LSB
MSB
LSB
MSB
: INVALID

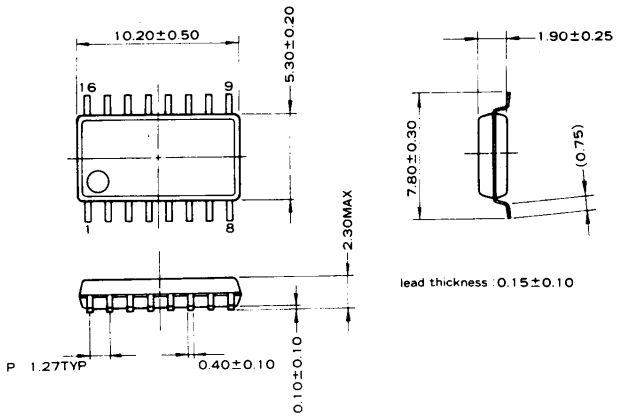
■ EXTERNAL DIMENSIONS

(1)YSF224B-D



Plastic body dimensions do not include burr of resin.
UNIT: mm

(2)YSF224B-M



The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

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