

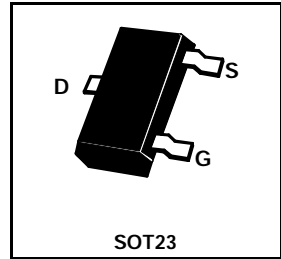
SOT23 N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ISSUE 3 – MARCH 1996



BSS138

PARTMARKING DETAIL - SS



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	50	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	I_D	200	mA
Pulsed Drain Current	I_{DM}	800	mA
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation at $T_{amb}=25^{\circ}C$	P_{tot}	360	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

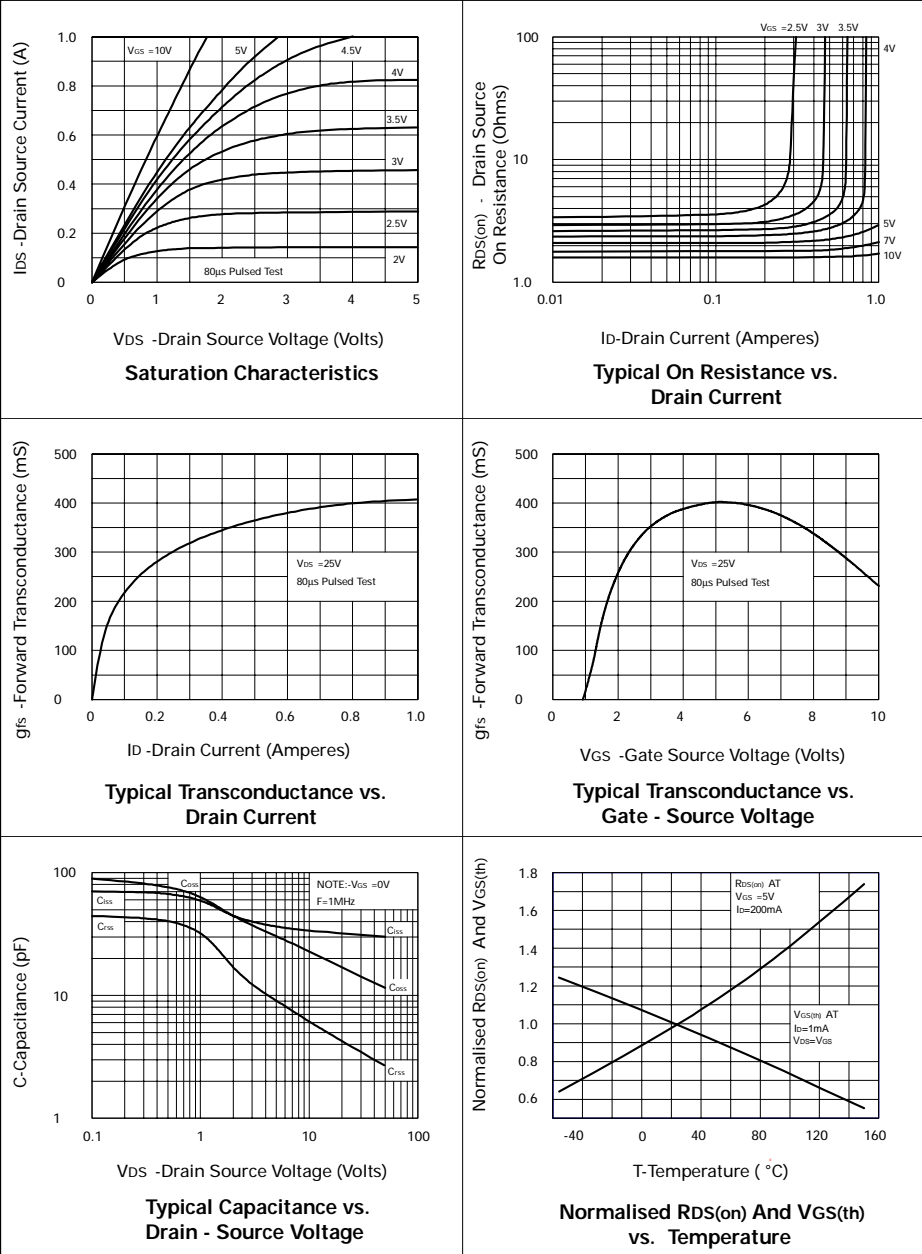
PARAMETER	SYMBOL	MIN.	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	50			V	$I_D=0.25mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.5		1.5	V	$I_D=1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	I_{GSS}			100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}			0.5 5 100	μA μA nA	$V_{DS}=50V, V_{GS}=0$ $V_{DS}=50V, V_{GS}=0V, T=125^{\circ}C(2)$ $V_{DS}=20V, V_{GS}=0$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			3.5	Ω	$V_{GS}=5V, I_D=200mA$
Forward Transconductance(1)(2)	g_{fs}	120			mS	$V_{DS}=25V, I_D=200mA$
Input Capacitance (2)	C_{iss}			50	pF	$V_{DS}=25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	C_{oss}			25	pF	
Reverse Transfer Capacitance (2)	C_{rss}			8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		10		ns	$V_{DD}=30V, I_D=280mA$
Rise Time (2)(3)	t_r		10		ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		15		ns	
Fall Time (2)(3)	t_f		25		ns	

(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.

(3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator

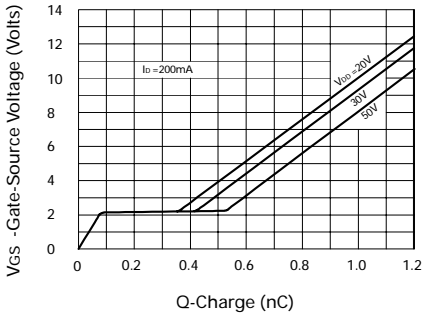
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TYPICAL CHARACTERISTICS

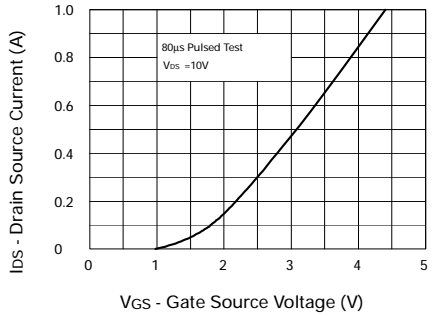


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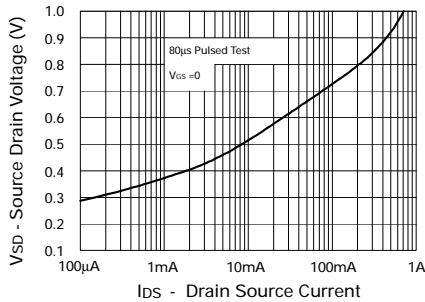
TYPICAL CHARACTERISTICS



Typical Gate Charge vs. Gate-Source Voltage



Typical Transfer Characteristics



Typical Diode Forward Voltage