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**LCD BIAS BOOST CONVERTER****DESCRIPTION**

The ZXLB1600 DC/DC boost converter accepts an input voltage of between 1.6V and 5.5V and provides an adjustable output voltage of up to 28V for LCD backplane bias. The device contains the output switch and a second switch to isolate the coil from the input and provide true isolation in shutdown mode. The output can be adjusted by means of an externally applied dc voltage, or PWM control signal and can supply typically 10mA of output current at maximum output voltage. Higher current is available at lower output voltages.

The input voltage range accepts a number of battery solutions, including dual dry cell and single Li-Ion cells and PFM operation mode allows the output to be regulated with high efficiency under light or no load conditions. The switching frequency range permits the use of miniature surface mount inductors.

The voltage control range can be modified, if required, by external resistors. A low battery comparator is provided to indicate when the input voltage has fallen to within  $\pm 2\%$  of a preset threshold.

**FEATURES**

- Wide input voltage range: 1.6 to 5.5V
- Adjustable output voltage up to 28V using PWM or analog control voltage
- True shutdown (output isolated from input)
- Internal output switch and current sense
- Low quiescent current: (75 $\mu$ A max)
- 5 $\mu$ A (max) shutdown current (including low battery comparator)
- Up to 500kHz switching frequency (PFM)
- 85% efficiency
- Low battery flag
- Small MSOP10 package
- Low external component count

**APPLICATIONS**

- PDAs
- Mobile Phones
- Digital Cameras
- Portable Internet Appliances
- Notebook and Palmtop computers

**ORDERING INFORMATION**

DEVICE	DEVICE DESCRIPTION	TEMPERATURE RANGE	PART MARK	TAPING OPTIONS
ZXLB1600X10	Boost converter for LCD bias in MSOP10	0 °C to 70 °C	ZXLB1600	TA, TC

**TA reels 500 devices, TC reels 2500 devices**

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# ZXLB1600

## ABSOLUTE MAXIMUM RATINGS

(Voltages to GND unless otherwise stated)

Output Voltage	30V
Input Voltage	7V
Switch output current	500mA
Power Dissipation	800mW
Operating Temperature	0 to 70°C
Storage Temperature	-55 to 125°C
Junction Temperature	150°C

## ELECTRICAL CHARACTERISTICS:

Test conditions unless otherwise stated:  $V_{IN}=3.0V$ ,  $T_{AMB}=25^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>General</b>						
$V_{IN}$	Input voltage		1.6	3	5.5	V
$I_{IN}$	Supply current	$V_{EN} = 0V$ , $V_{IN} = 5.5V$ (Note 1) $V_{EN} = V_{IN}$ , $I_{OUT} = 0V$		3	5	$\mu A$
	Shutdown Quiescent				75	$\mu A$
<b>Isolating switch</b>						
$R_{ISO}$	'On' resistance	$V_{EN} = V_{IN}$		0.8	2	$\Omega$
$I_{ISO}$	Leakage current	$V_{EN} = 0V$			1	$\mu A$
<b>LX Switch</b>						
$I_{LX}$	Switch peak current limit		0.2	0.3	0.5	A
$R_{LX}$	'On' resistance			1.0	2	$\Omega$
$I_{LX(leak)}$	Switch leakage current				1	$\mu A$
<b>Controller output</b>						
$V_{OUT}$	Output voltage range		$V_{IN}$		29	V
$I_{OUT}$	Maximum output current	$LX = 22\mu H$ , $V_{OUT} = 28V$	5	10		mA
$\Delta V_{LNR}$	Line regulation	$I_{OUT} = 1mA$ , $2V < V_{IN} < 5.5V$		0.1		%/V
$\Delta V_{LDR}$	Load regulation	$V_{OUT} = 28V$ , $100\mu A < I_{OUT} < 5mA$		0.01		%/mA
$f_{LX}$	Operating frequency			200	500	kHz
$T_{ON}$	Output 'ON' time	LX output low			10	$\mu s$
$T_{OFF}$	Output 'OFF' time	LX output off	1			$\mu s$
$\xi$	Efficiency	$V_{OUT} = 28V$ , $I_{OUT} = 1mA$ , $L=22\mu H$		85		%

Note:1 Shutdown current includes 3 $\mu A$  (max) for the battery low comparator, which remains active in shutdown mode

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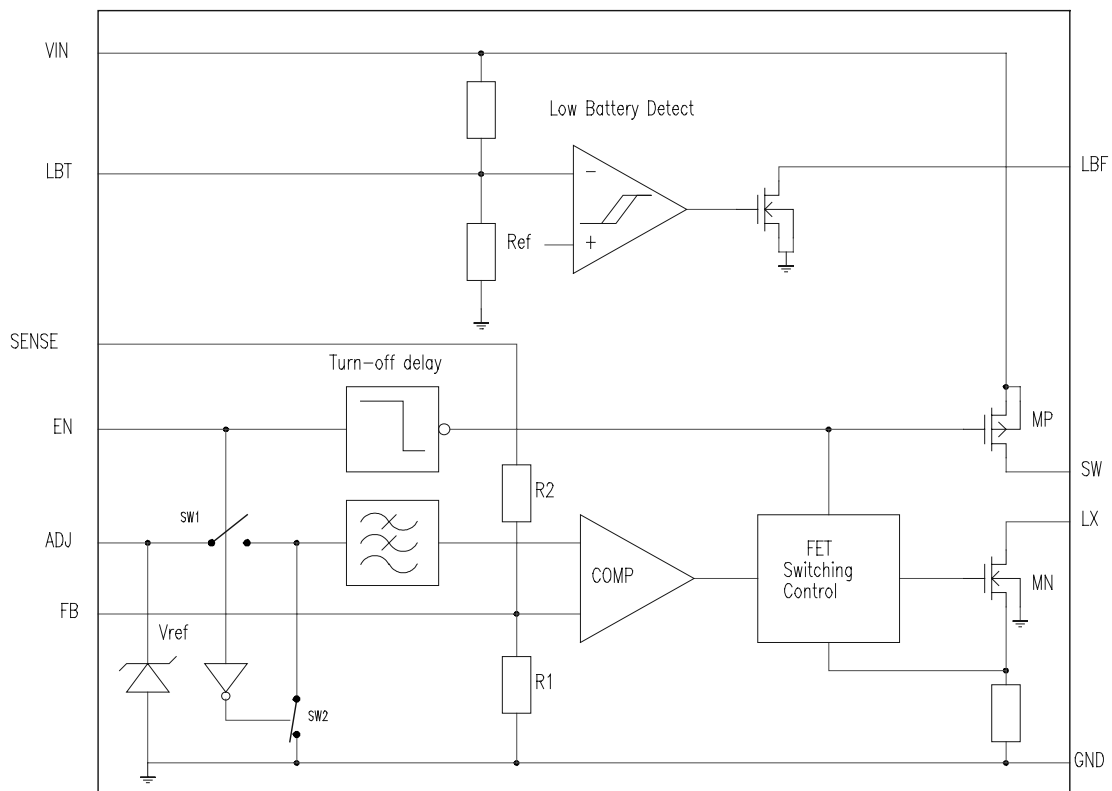
Test conditions unless otherwise stated:  $V_{IN}=3.0V$ ,  $T_{AMB}=25^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Output Voltage control by dc voltage applied to 'ADJ' pin</b>						
$V_{ADJ(NOM)}$ $V_{ADJ}$	Internal reference voltage External overdrive voltage range on 'ADJ' pin for output voltage control	'ADJ' pin floating, 'EN' = $V_{IN}$	0.5	1.23	$V_{ADJ(NOM)}$	V V
$I_{ADJ}$	Input current	$0.5 < V_{ADJ} < V_{ADJ(NOM)}$			-10	$\mu A$
$V_{SENSE}$	Output voltage	'ADJ' pin floating, 'EN' = $V_{IN}$	27		29	V
<b>Output Voltage control by PWM signal applied to 'EN' input</b>						
$\Delta T/T$	PWM duty cycle range at 'EN' input	$10kHz < f < 100kHz$ , $V_{ENH} = V_{IN}$	40		100	%
$f_{LPF}$	Internal low pass filter cut-off frequency			4		kHz
$A_{LPF}$	Filter attenuation	$F=30kHz$		52.5		dB
<b>Enable input</b>						
$V_{ENL}$	Low level Input voltage	Device in shutdown			0.4	V
$V_{ENH}$	High level Input voltage	Device active	1.4		$V_{in}$	V
$I_{ENL}$	Low level input current	$V_{EN} = 0V$			-100	nA
$I_{ENH}$	High level input current	$V_{EN} = V_{IN}$			100	nA
<b>Battery low comparator</b>						
$I_{BLQ}$	Quiescent current	$V_{IN} = 5.5V$			3	$\mu A$
$V_{BLT}$	Detection threshold	$V_{IN}$ falling		2		V
$V_{BTOL}$	Threshold tolerance				+/-2	%
$V_{BLHYS}$	Hysteresis	$V_{IN}$ rising		20		mV
$V_{LBT}$	Threshold voltage on LBT pin	LBT floating		1.21		V
$V_{LBT(max)}$	Maximum voltage on LBT pin during normal device operation				$V_{in} - 0.5$	V
$I_{BLOL}$	Low level output current	Output 'on'			1	mA
$V_{BLOL}$	Low level output voltage	$I_{BLOL} = 1mA$			0.4	V
$I_{BLOH}$	High level output current	Output 'off'			2	$\mu A$
$V_{BLOH}$	High level output voltage	Output 'off'			29	V

## PIN DESCRIPTION

Pin #	Name	Description
1	ADJ	Internal or external reference voltage
2	EN	Enable input (active high) Also used to adjust output voltage by PWM signal
3	VIN	Input voltage
4	SW	Output of high side PMOS isolation switch
5	SENSE	Output voltage sense
6	LX	Output of NMOS switch
7	LBF	Low Battery Flag output: open drain (active low for low battery voltage) Remains active when EN is high
8	GND	Ground
9	FB	Voltage Feedback pin for output (threshold 1.23V)
10	LBT	Low Battery flag Threshold adjust input (threshold 1.21V)

## BLOCK DIAGRAM



## Device Description

The device is a flyback boost regulator, working in discontinuous mode.

## Device Operation

With reference to the chip block diagram and typical application circuit:

### Control loop operation

When 'EN' is high, the control circuits become active. The high side of the coil is connected to the input via a large PMOS isolating switch (MP) and the low side to ground via a NMOS transistor (MN). The current in the coil is allowed to build up to an internally defined level (nominally 300mA) before MN is turned off. The energy stored in the coil is then transferred to the output capacitor (C1) via a Schottky diode (SD). The output voltage is sensed at pin 'SENSE' by internal resistors R1 and R2 (which may be shunted externally at pin 'FB') and compared to a reference voltage (1.23V nominal). A comparator senses when the output voltage is above that set by the reference and its output is used to control the 'off' time of the output switch. The control loop is self-oscillating, producing fixed pulses of 10us maximum width, at a frequency that varies in proportion to the output load current. This mode of operation is known as Pulse Frequency Modulation (PFM)

### Setting output voltage

The output voltage is equal to the voltage present on the 'ADJ' pin of the device multiplied by the internal resistor network factor  $(R1+R2)/R1$ . The ADJ pin is connected to the internal reference voltage of value  $V_{ADJ(NOM)}$ , and by default will give a nominal output of 28V. However, if required, the ADJ pin may be overdriven with an external dc voltage, in order to adjust the output voltage to a value lower than the default value.

The reference voltage on the ADJ pin is switched into a low pass filter circuit when the EN pin is high and the output of this filter drives the comparator within the control loop. By varying the duty cycle of the EN signal, the control loop will see a voltage, which has an average value equal to the duty cycle multiplied by the voltage present on the ADJ pin. This provides an alternative means of adjusting the output voltage. It also allows the device to be both turned on and adjusted with a single signal at the 'EN' pin. The output voltage during this mode of operation will be  $V_{ADJ} \times (R1+R2)/R1 \times \text{duty cycle}$ .

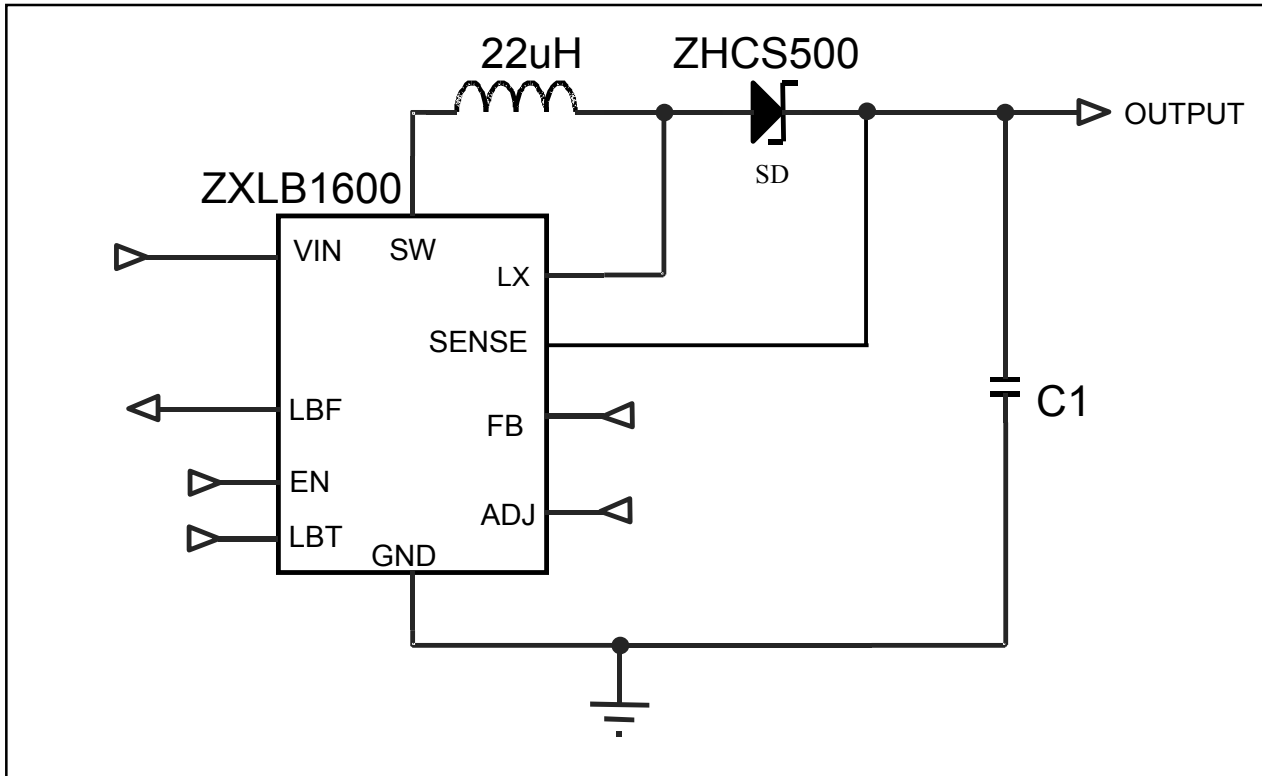
To reduce standby current consumption, the internal reference is turned off when no signal is present on the 'EN' pin

Further control over output voltage during either mode of operation is possible by shunting the internal resistor network comprising R1 and R2 by means of external resistors connected to the SENSE and FB pins.

### Low Battery detection

A comparator driving an open drain NMOS output transistor performs the low battery flag function. The detection threshold (battery voltage falling) is set internally to 2V nominal, but this can be changed by shunting the internal potential divider with two external resistors at pin 'LBT'. Operation is such that the output transistor will be turned on when the battery voltage falls below the detection threshold. A small amount (nominal 20mV) of hysteresis is provided to aid clean switching. The low battery detect circuit remains active when 'EN' is low.

## TYPICAL APPLICATION CIRCUIT



### APPLICATION NOTES

#### Increased efficiency

If the isolation of the coil from the supply is not needed, the SW pin can be connected to VIN to improve efficiency. This prevents power loss in the internal high-side PMOS switch.

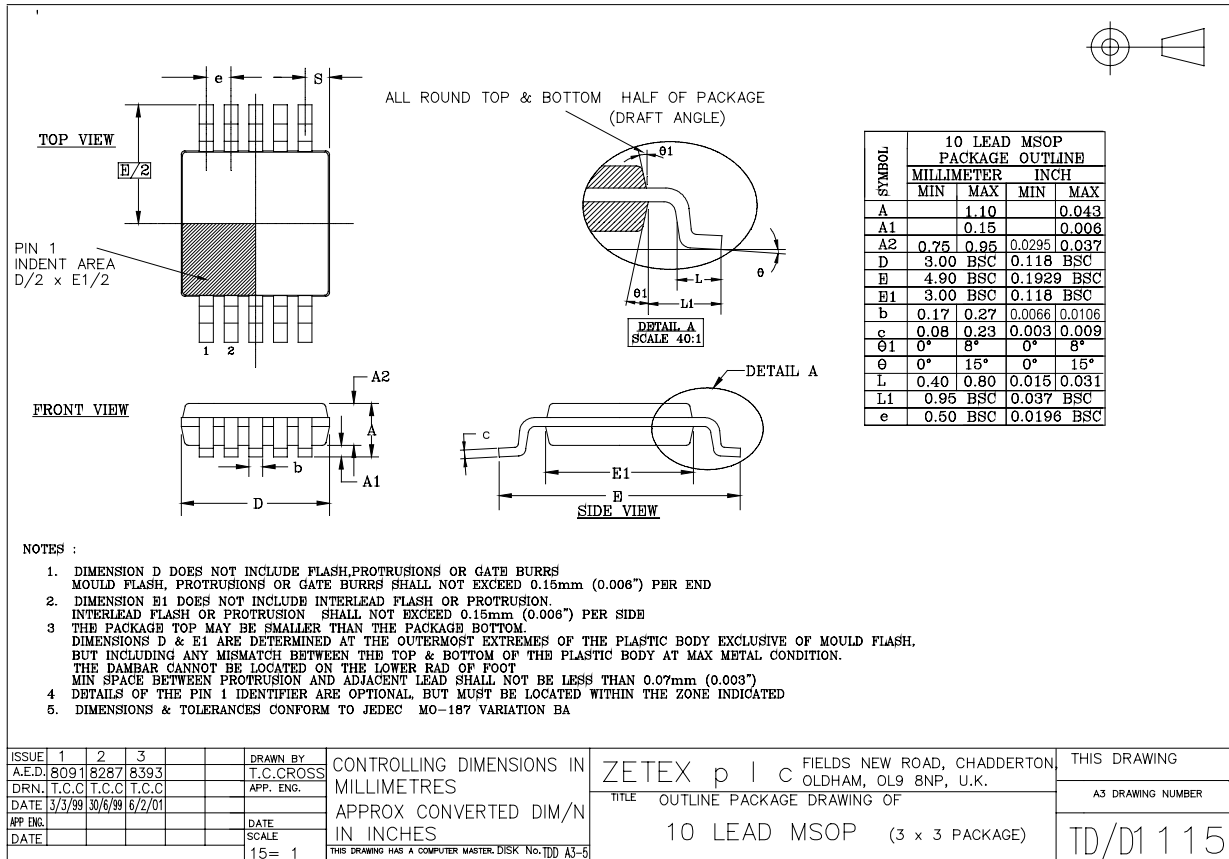
#### Low Battery Flag Output, LBF

This is an open drain output that switches low when the battery voltage falls below the detection threshold. An external pull-up resistor can be connected to this pin to allow it to interface to any voltage up to a maximum of 29V.

#### Layout considerations

The FB and LBT pins are high impedance inputs, so PCB track lengths to these should be kept as short as possible. A small capacitor (~100pF) can be connected from the FB pin to the output to reduce output ripple and noise. Also a capacitor can be connected from the LBT pin to ground to minimise noise pickup into the low battery comparator if required.

## PACKAGE OUTLINE



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