



# Z86E73/E74 32K OTP Z86L73/L74 32K ROM INFRARED REMOTE CONTROLLERS

## FEATURES

Part	ROM (Kbyte)	RAM* (Kbyte)	One-Time Programmable	Speed (MHz)
Z86E73	32	1004	Yes	8
Z86L73	32	492	No	8
Z86E74	32	1004	Yes	8
Z86L74	32	1004	No	8

\* General-Purpose

- 40-Pin DIP, 44-Pin PLCC/QFP Packages (E73/L73)  
64-Pin DIP, 68-Pin PLCC Packages (E74/L74)
- 2.0V to 3.9V Operating Range (L73/L74)  
4.5V to 5.5V Operating Range (E73/E74)
- Low-Power Consumption  
(Typical: 40 mw for L73/L74)  
(Typical: 60 mw for E73/E74)
- 0°C to +70°C Temperature Range

- Expanded Register Files (ERF)
- 31 Input/Output Lines (E73/L73)  
51 Input/Output Lines (E74/L74\*)  
**\*Note: With Auto Latch on Port 4, 5 and 6.**
- Five Prioritized Interrupts with Programmable Polarity
- Two Comparators
- 8-Bit Counter/Timer with Two Capture Registers and  
16-Bit Counter/Timer with One Capture Register
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- On-Chip Oscillator that Accepts a Crystal, Ceramic  
Resonator, LC, RC, or External Clock Drive
- Low-Voltage Detection and Protection
- 32-KHz Mask Option to Disable Internal Feedback  
Resistor (L73/L74)

## GENERAL DESCRIPTION

The Z86E73/L73/E74/L74 are ROM-based members of Zilog's Z8® single-chip microcontroller family of infrared (IR) consumer controller processors featuring fast and flexible code execution. The Z86E73/E74 devices offer a one-time programmable (OTP) option.

For applications demanding powerful I/O capabilities, the Z86E73/L73's dedicated input and output lines are grouped into four ports, and into seven ports for the Z86E74/L74. They are configurable under software control to provide timing, status signals, or parallel I/O.

Four address spaces, the Program Memory, Register File, Data Memory, and Expanded Register File (ERF) support a wide range of memory configurations. Through the ERF the designer has access to three additional control registers that provide extra peripheral devices, I/O ports, and register addresses.

Two on-chip counter/timers, with a large number of selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O datacommunications.

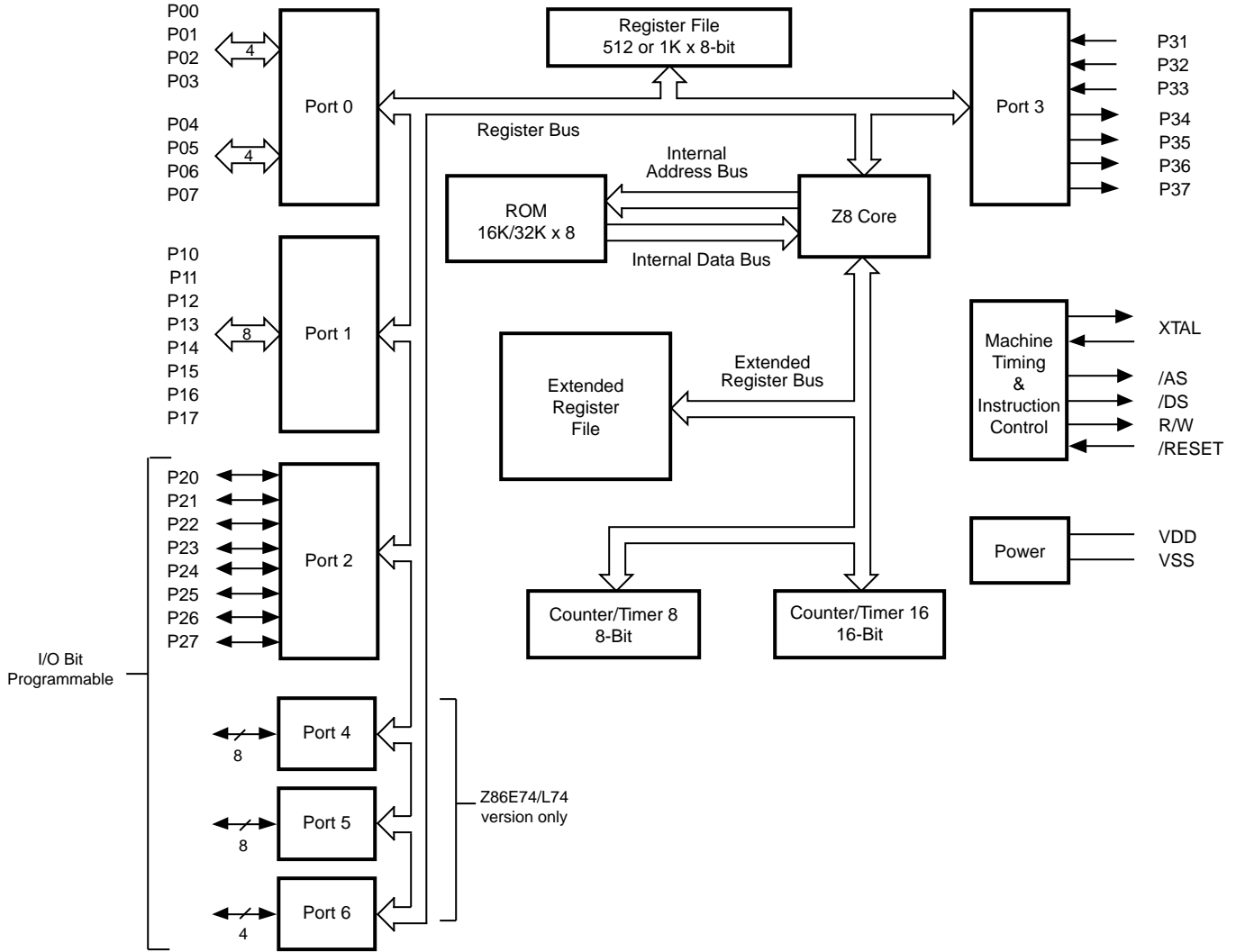
### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

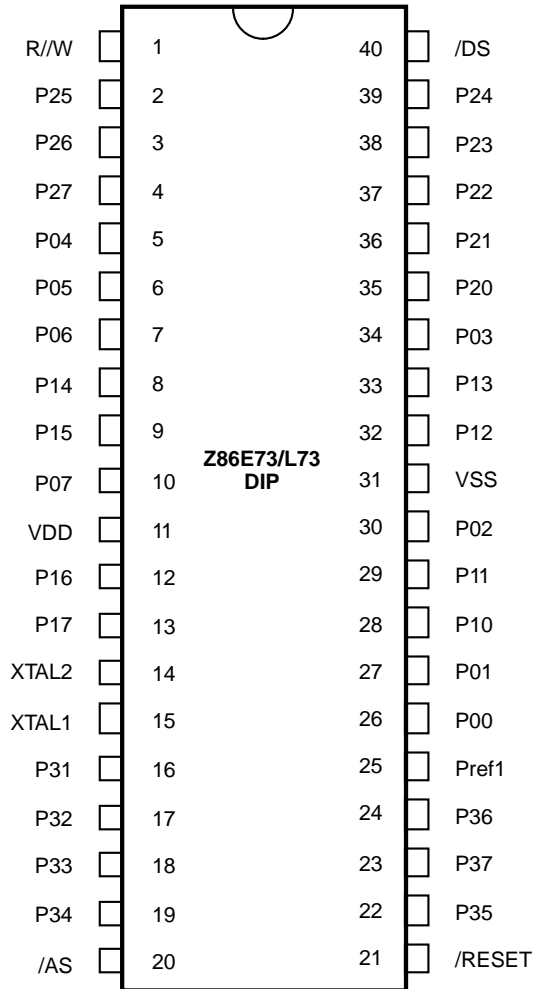
Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

GENERAL DESCRIPTION (Continued)

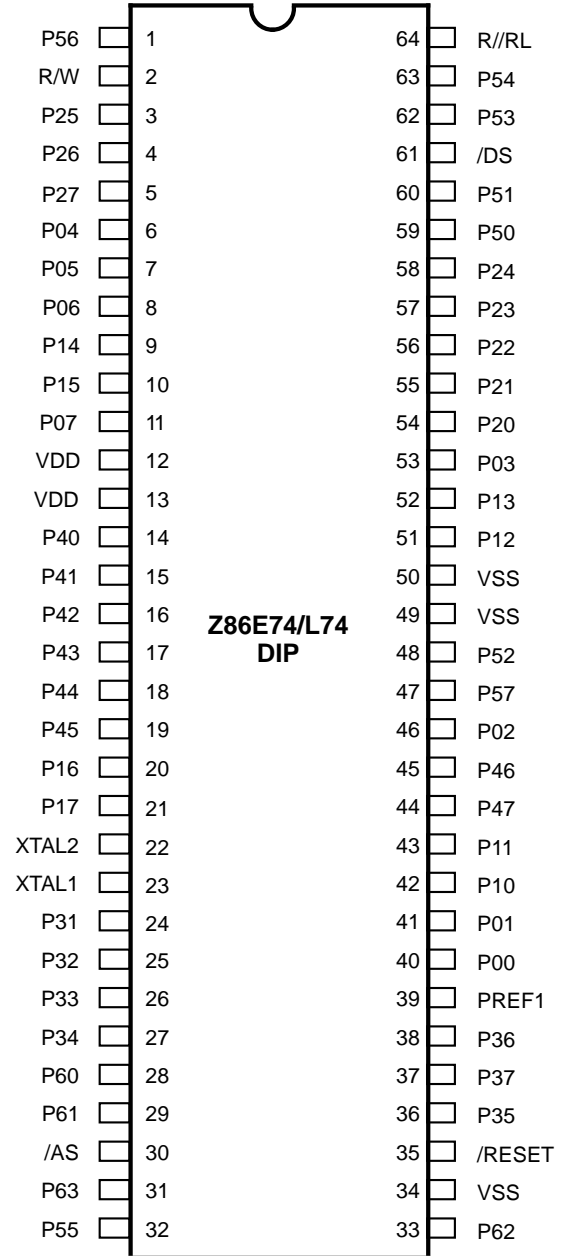


Functional Block Diagram

**PIN DESCRIPTION**

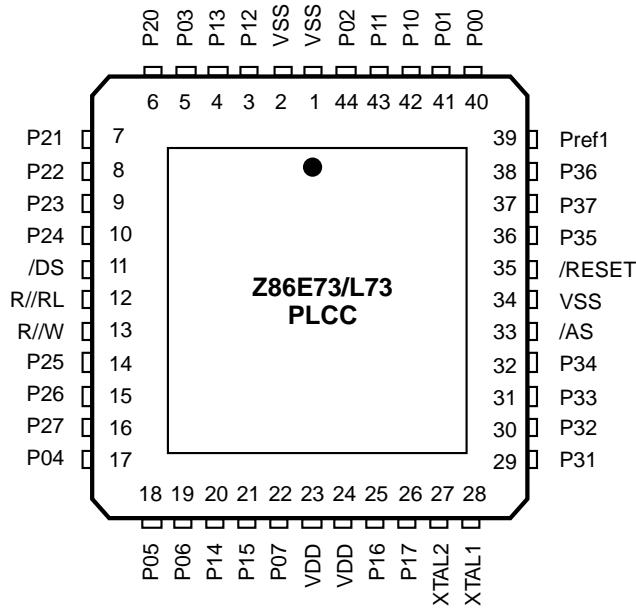


**Z86E73 (Standard Mode)  
Z86L73 40-Pin DIP  
Pin Assignments**

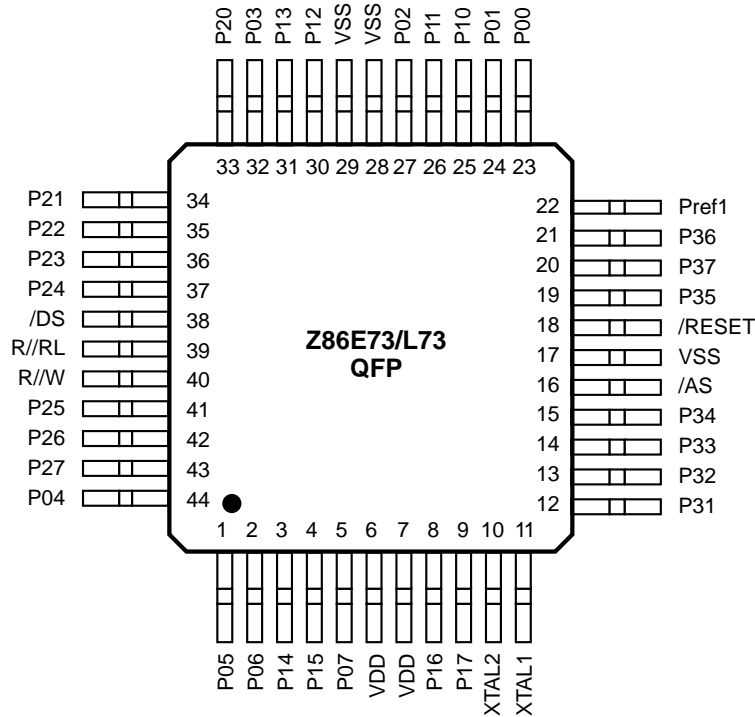


**Z86E74 (Standard Mode)  
Z86L74 64-Pin DIP  
Pin Assignments**

PIN DESCRIPTION

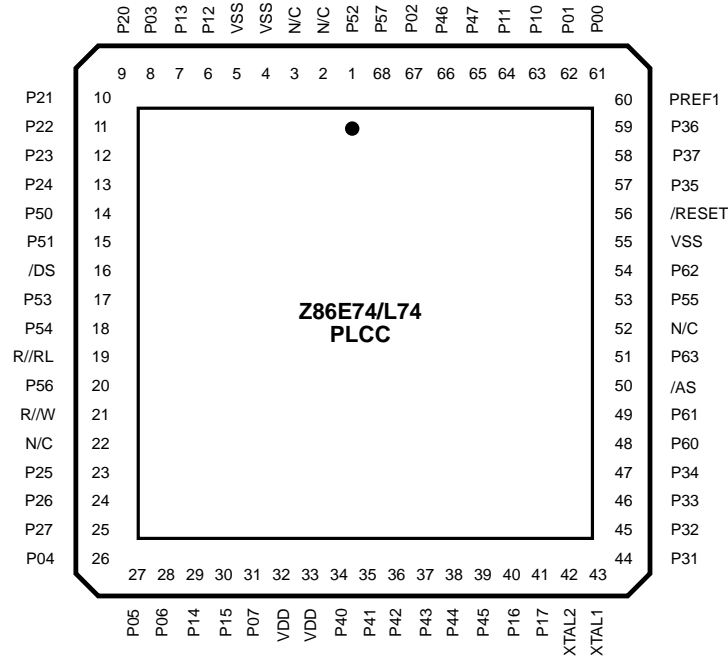


**Z86E73 (Standard Mode)  
Z86L73 44-Pin PLCC  
Pin Assignments**



**Z86E73 (Standard Mode)  
Z86L73 44-Pin QFP  
Pin Assignments**

PIN DESCRIPTION (Continued)



**Z86E74 (Standard Mode)  
Z86L74 68-Pin PLCC Pin Assignments**

## ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply Voltage (*)	-0.3	+7.0	V
$T_{STG}$	Storage Temp.	-65°	+150°	C
$T_A$	Oper. Ambient Temp.		†	C

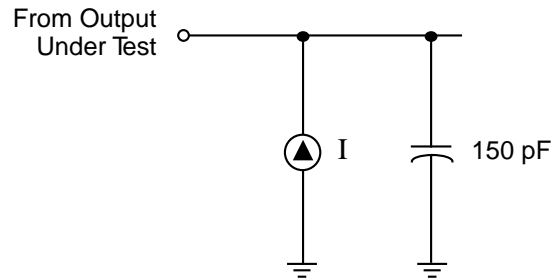
**Notes:**

\* Voltage on all pins with respect to GND.  
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).



**Test Load Diagram**

## CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ ,  $f = 1.0\text{ MHz}$ , unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

**DC CHARACTERISTICS (Z86E73/E74)**

Sym	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes [3]
			Min	Max				
V <sub>CH</sub>	Max Input Voltage	4.0V		7		V	I <sub>IN</sub> = 250 μA	
		5.5V		7		V	I <sub>IN</sub> = 250 μA	
	Clock Input High Voltage	4.0V	0.9 V <sub>CC</sub>	V <sub>CC</sub> + 0.3		V	Driven by External Clock Generator	
		5.5V	0.9 V <sub>CC</sub>	V <sub>CC</sub> + 0.3		V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	4.0V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>		V	Driven by External Clock Generator	
		5.5V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>		V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	4.0V	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	1.3	V		
		5.5V	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	2.5	V		
V <sub>IL</sub>	Input Low Voltage	4.0V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.5	V		
		5.5V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.9	V		
V <sub>OH1</sub>	Output High Voltage	4.0V	V <sub>CC</sub> - 0.4		1.7	V	I <sub>OH</sub> = -0.5 mA	
		5.5V	V <sub>CC</sub> - 0.4		3.7	V	I <sub>OH</sub> = -0.5 mA	
V <sub>OH2</sub>	Output High Voltage (P36, P37)	4.0V	0.7			V	I <sub>OH</sub> = -7 mA	[10]
		5.5V	0.7			V	I <sub>OH</sub> = -7 mA	[10]
V <sub>OL1</sub>	Output Low Voltage	4.0V		0.4	0.2	V	I <sub>OL</sub> = 1.0 mA	
		5.5V		0.4	0.1	V	I <sub>OL</sub> = 4.0 mA	
V <sub>OL2</sub>	Output Low Voltage	4.0V		0.8	0.3	V	I <sub>OL</sub> = 2.0 mA 3 Pin Max	
		5.5V		0.8	0.5	V	I <sub>OL</sub> = 8.0 mA 3 Pin Max	
V <sub>OL2</sub>	Output Low Voltage (P20-P22, P36, P00, P01, P07)	4.0V		0.8	0.3	V	I <sub>OL</sub> = 10 mA	[9]
		5.5V		0.8	0.5	V	I <sub>OL</sub> = 10 mA 2 O/P only	[9]
V <sub>RH</sub>	Reset Input High Voltage	4.0V	0.8 V <sub>CC</sub>	V <sub>CC</sub>	1.5	V		
		5.5V	0.8 V <sub>CC</sub>	V <sub>CC</sub>	3.0	V		
V <sub>RI</sub>	Reset Input Low Voltage	4.0V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.5			
		5.5V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.9			
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	4.0V		25	10	mV		
		5.5V		25	10	mV		
I <sub>IL</sub>	Input Leakage	4.0V	-1	1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		5.5V	-1	1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>OL</sub>	Output Leakage	4.0V	-1	1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		5.5V	-1	1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>IR</sub>	Reset Input Current	4.0V		-45	-20	μA		
		5.5V		-55	-30	μA		
I <sub>CC</sub>	Supply Current	4.0V		10	4	mA	@ 8.0 MHz	[4, 5]
		5.5V		15	10	mA	@ 8.0 MHz	[4, 5]
		4.0V		100	10	μA	@ 32 kHz	[4, 5,11]
		5.5V		300	10	μA	@ 32 kHz	[4, 5,11]

**DC CHARACTERISTICS (Z86E73/E74) (Continued)**

Sym	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes [3]
			Min	Max				
I <sub>CC1</sub>	Standby Current	4.0V		3	1	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8.0 MHz	[4,5]
		5.5V		5	4	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8.0 MHz	[4,5]
		4.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
		5.5V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
I <sub>CC2</sub>	Standby Current	4.0V		8	2	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	[6,8]
		5.5V		10	3	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	[6,8]
		4.0V		500	310	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is Running	[6,8]
		5.5V		800	600	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is Running	[6,8]
T <sub>POR</sub>	Power-On Reset	4.0V	15	75	13	ms		
		5.5V	5	20	7	ms		
V <sub>LV</sub>	V <sub>CC</sub> Low Voltage Protection			3.3	2.75	V	8 MHz max Ext. CLK Freq.	[7]

**Notes:**

- | [1] | I <sub>CC1</sub>     | Typ    | Max | Unit | Frequency |
|-----|----------------------|--------|-----|------|-----------|
|     | Crystal/Resonator    | 3.0 mA | 5   | mA   | 8.0 MHz   |
|     | External Clock Drive | 0.3 mA | 5   | mA   | 8.0 MHz   |
- [2] GND = 0V.  
 [3] 4.0V to 5.5V.  
 [4] All outputs unloaded, I/O pins floating, inputs at rail.  
 [5] CL1 = CL2 = 100 pF.  
 [6] Same as note [4] except inputs at V<sub>CC</sub>.  
 [7] The V<sub>LV</sub> increases as the temperature decreases.  
 [8] Oscillator stopped.  
 [9] Two outputs at a time, independent to other outputs.  
 [10] One at a time.  
 [11] 32 kHz clock driver input.



**DC CHARACTERISTICS (Z86L73/L74)**

Sym	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes [3]
			Min	Max				
V <sub>CH</sub>	Max Input Voltage	2.0V		7		V	I <sub>IN</sub> = 250 μA	
		3.9V		7		V	I <sub>IN</sub> = 250 μA	
	Clock Input High Voltage	2.0V	0.9 V <sub>CC</sub>	V <sub>CC</sub> + 0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V <sub>CC</sub>	V <sub>CC</sub> + 0.3		V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>		V	Driven by External Clock Generator	
		3.9V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>		V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0V	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	1.3	V		
		3.9V	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	2.5	V		
V <sub>IL</sub>	Input Low Voltage	2.0V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.5	V		
		3.9V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.9	V		
V <sub>OH1</sub>	Output High Voltage	2.0V	V <sub>CC</sub> - 0.4		1.7	V	I <sub>OH</sub> = -0.5 mA	
		3.9V	V <sub>CC</sub> - 0.4		3.7	V	I <sub>OH</sub> = -0.5 mA	
V <sub>OH2</sub>	Output High Voltage (P36, P37)	2.0V	0.7			V	I <sub>OH</sub> = -7 mA	[10]
		3.9V	0.7			V	I <sub>OH</sub> = -7 mA	[10]
V <sub>OL1</sub>	Output Low Voltage	2.0V		0.4	0.2	V	I <sub>OL</sub> = 1.0 mA	
		3.9V		0.4	0.1	V	I <sub>OL</sub> = 4.0 mA	
V <sub>OL2</sub>	Output Low Voltage	2.0V		0.8	0.3	V	I <sub>OL</sub> = 2.0 mA 3 Pin Max	
		3.9V		0.8	0.5	V	I <sub>OL</sub> = 8.0 mA 3 Pin Max	
V <sub>OL2</sub>	Output Low Voltage (P20-P22, P36, P00, P01, P07)	2.0V		0.8	0.3	V	I <sub>OL</sub> = 10 mA	[9]
		3.9V		0.8	0.5	V	I <sub>OL</sub> = 10 mA 2 O/P only	[9]
V <sub>RH</sub>	Reset Input High Voltage	2.0V	0.8 V <sub>CC</sub>	V <sub>CC</sub>	1.5	V		
		3.9V	0.8 V <sub>CC</sub>	V <sub>CC</sub>	3.0	V		
V <sub>RI</sub>	Reset Input Low Voltage	2.0V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.5			
		3.9V	V <sub>SS</sub> - 0.3	0.2 V <sub>CC</sub>	0.9			
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
I <sub>IL</sub>	Input Leakage	2.0V	-1	1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		3.9V	-1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>		
I <sub>OL</sub>	Output Leakage	2.0V	-1	1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		3.9V	-1	1	< 1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>IR</sub>	Reset Input Current	2.0V		-45	-20	μA		
		3.9V		-55	-30	μA		
I <sub>CC</sub>	Supply Current	2.0V		10	4	mA	@ 8.0 MHz	[4, 5]
		3.9V		15	10	mA	@ 8.0 MHz	[4, 5]
		2.0V		100	10	μA	@ 32 kHz	[4, 5, 11]
		3.9V		300	10	μA	@ 32 kHz	[4, 5, 11]

**DC CHARACTERISTICS (Z86L73/L74)** (Continued)

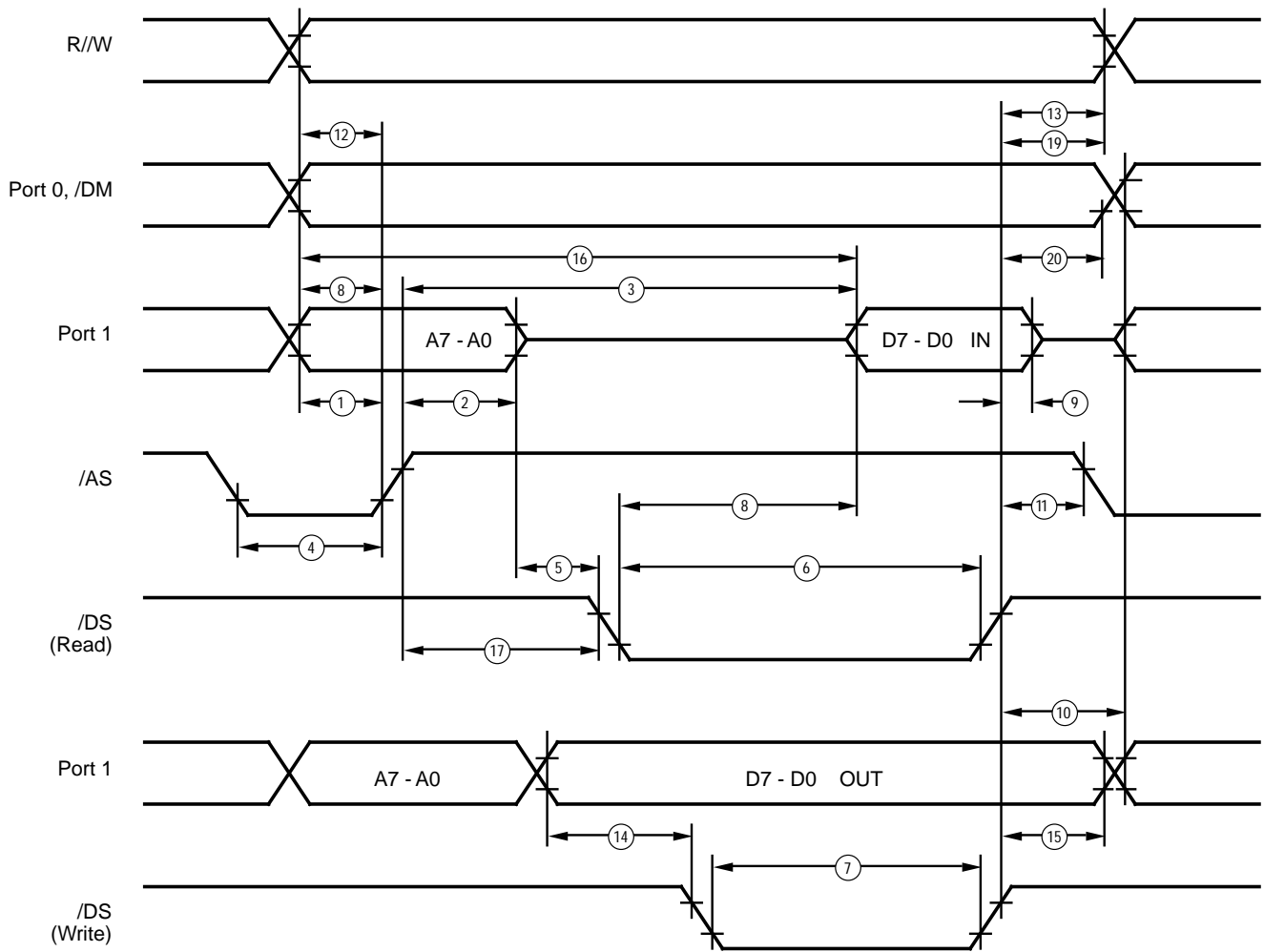
Sym	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes [3]
			Min	Max				
I <sub>CC1</sub>	Standby Current	2.0V		3	1	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8.0 MHz	[4,5]
		3.9V		5	4	mA	HALT Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> @ 8.0 MHz	[4,5]
		2.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
		3.9V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
I <sub>CC2</sub>	Standby Current	2.0V		8	2	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	[6,8]
		3.9V		10	3	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is not Running	[6,8]
		2.0V		500	310	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is Running	[6,8]
		3.9V		800	600	μA	STOP Mode V <sub>IN</sub> = 0V, V <sub>CC</sub> WDT is Running	[6,8]
T <sub>POR</sub>	Power-On Reset	2.0V	15	75	13	ms		
		3.9V	5	20	7	ms		
V <sub>LV</sub>	V <sub>CC</sub> Low Voltage Protection			2.15	1.7	V	8 MHz max Ext. CLK Freq.	[7]

**Notes:**

- | [1] | I <sub>CC1</sub>     | Typ    | Max | Unit | Frequency |
|-----|----------------------|--------|-----|------|-----------|
|     | Crystal/Resonator    | 3.0 mA | 5   | mA   | 8.0 MHz   |
|     | External Clock Drive | 0.3 mA | 5   | mA   | 8.0 MHz   |
- [2] GND = 0V.  
 [3] 2.0V to 3.9V.  
 [4] All outputs unloaded, I/O pins floating, inputs at rail.  
 [5] CL1 = CL2 = 100 pF.  
 [6] Same as note [4] except inputs at V<sub>CC</sub>.  
 [7] The V<sub>LV</sub> increases as the temperature decreases.  
 [8] Oscillator stopped.  
 [9] Two outputs at a time, independent to other outputs.  
 [10] One at a time.  
 [11] 32 kHz clock driver input.

**AC CHARACTERISTICS**

External I/O or Memory Read and Write Timing Diagram



**External I/O or Memory Read/Write Timing**

### AC CHARACTERISTICS (Z86E73/E74)

#### External I/O or Memory Read and Write Timing Table

No.	Symbol	Parameter	V <sub>CC</sub> Note [3]	T <sub>A</sub> = 0°C to +70°C 8.0 MHz		Units	Notes
				Min	Max		
1	TdA(AS)	Address Valid to /AS Rising Delay	4.0V	55		ns	[2]
			5.5V	55		ns	
2	TdAS(A)	/AS Rising to Address Float Delay	2.0V	70		ns	[2]
			5.5V	70		ns	
3	TdAS(DR)	/AS Rising to Read Data Required Valid	4.0V 5.5V		400 400	ns ns	[1, 2]
4	TwAS	/AS Low Width	4.0V	80		ns	[2]
			5.5V	80		ns	
5	Td	Address Float to /DS Falling	4.0V 5.5V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	4.0V	300		ns	[1, 2]
			5.5V	300		ns	
7	TwDSW	/DS (Write) Low Width	4.0V	165		ns	[1, 2]
			5.5V	165		ns	
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	4.0V		260	ns	[1, 2]
			5.5V		260	ns	
9	ThDR(DS)	Read Data to /DS Rising Hold Time	4.0V 5.5V	0 0		ns ns	[2]
10	TdDS(A)	/DS Rising to Address Active Delay	4.0V	85		ns	[2]
			5.5V	95		ns	
11	TdDS(AS)	/DS Rising to /AS Falling Delay	4.0V	60		ns	[2]
			5.5V	70		ns	
12	TdR/W(AS)	R/W Valid to /AS Rising Delay	4.0V	70		ns	[2]
			5.5V	70		ns	
13	TdDS(R/W)	/DS Rising to R/W Not Valid	4.0V	70		ns	[2]
			5.5V	70		ns	
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	4.0V	80		ns	[2]
			5.5V	80		ns	
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	4.0V	70		ns	[2]
			5.5V	80		ns	
16	TdA(DR)	Address Valid to Read Data Required Valid	4.0V		475	ns	[1, 2]
			5.5V		475	ns	
17	TdAS(DS)	/AS Rising to /DS Falling Delay	4.0V	100		ns	[2]
			5.5V	100		ns	
18	TdDM(AS)	/DM Valid to /AS Falling Delay	4.0V	55		ns	[2]
			5.5V	55		ns	
19	TdDS(DM)	/DS Rise to /DM Valid Delay	4.0V	70		ns	
			5.5V	70		ns	
20	ThDS(A)	/DS Rise to Address Valid Hold Time	4.0V	70		ns	
			5.5V	70		ns	

**Notes:**

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] 4.0V to 5.5V.

Standard Test Load.

All timing references use 0.9 V<sub>CC</sub> for a logic 1 and 0.1 V<sub>CC</sub> for a logic 0.

## AC CHARACTERISTICS (Z86L73/L74)

### External I/O or Memory Read and Write Timing Table

No.	Symbol	Parameter	V <sub>CC</sub> Note [3]	T <sub>A</sub> = 0°C to +70°C 8.0 MHz		Units	Notes
				Min	Max		
1	TdA(AS)	Address Valid to /AS Rising Delay	2.0V	55		ns	[2]
			3.9V	55		ns	
2	TdAS(A)	/AS Rising to Address Float Delay	2.0V	70		ns	[2]
			3.9V	70		ns	
3	TdAS(DR)	/AS Rising to Read Data Required Valid	2.0V		400	ns	[1, 2]
			3.9V		400	ns	
4	TwAS	/AS Low Width	2.0V	80		ns	[2]
			3.9V	80		ns	
5	Td	Address Float to /DS Falling	2.0V	0		ns	
			3.9V	0		ns	
6	TwDSR	/DS (Read) Low Width	2.0V	300		ns	[1, 2]
			3.9V	300		ns	
7	TwDSW	/DS (Write) Low Width	2.0V	165		ns	[1, 2]
			3.9V	165		ns	
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	2.0V		260	ns	[1, 2]
			3.9V		260	ns	
9	ThDR(DS)	Read Data to /DS Rising Hold Time	2.0V	0		ns	[2]
10	TdDS(A)	/DS Rising to Address Active Delay	2.0V	85		ns	[2]
			3.9V	95		ns	
11	TdDS(AS)	/DS Rising to /AS Falling Delay	2.0V	60		ns	[2]
			3.9V	70		ns	
12	TdR/W(AS)	R/W Valid to /AS Rising Delay	2.0V	70		ns	[2]
			3.9V	70		ns	
13	TdDS(R/W)	/DS Rising to R/W Not Valid	2.0V	70		ns	[2]
			3.9V	70		ns	
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	2.0V	80		ns	[2]
			3.9V	80		ns	
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	2.0V	70		ns	[2]
			3.9V	80		ns	
16	TdA(DR)	Address Valid to Read Data Required Valid	2.0V		475	ns	[1, 2]
			3.9V		475	ns	
17	TdAS(DS)	/AS Rising to /DS Falling Delay	2.0V	100		ns	[2]
			3.9V	100		ns	
18	TdDM(AS)	/DM Valid to /AS Falling Delay	2.0V	55		ns	[2]
			3.9V	55		ns	
19	TdDS(DM)	/DS Rise to /DM Valid Delay	2.0V	70		ns	
			3.9V	70		ns	
20	ThDS(A)	/DS Rise to Address Valid Hold Time	2.0V	70		ns	
			3.9V	70		ns	

**Notes:**

[1] When using extended memory timing add 2 TpC.

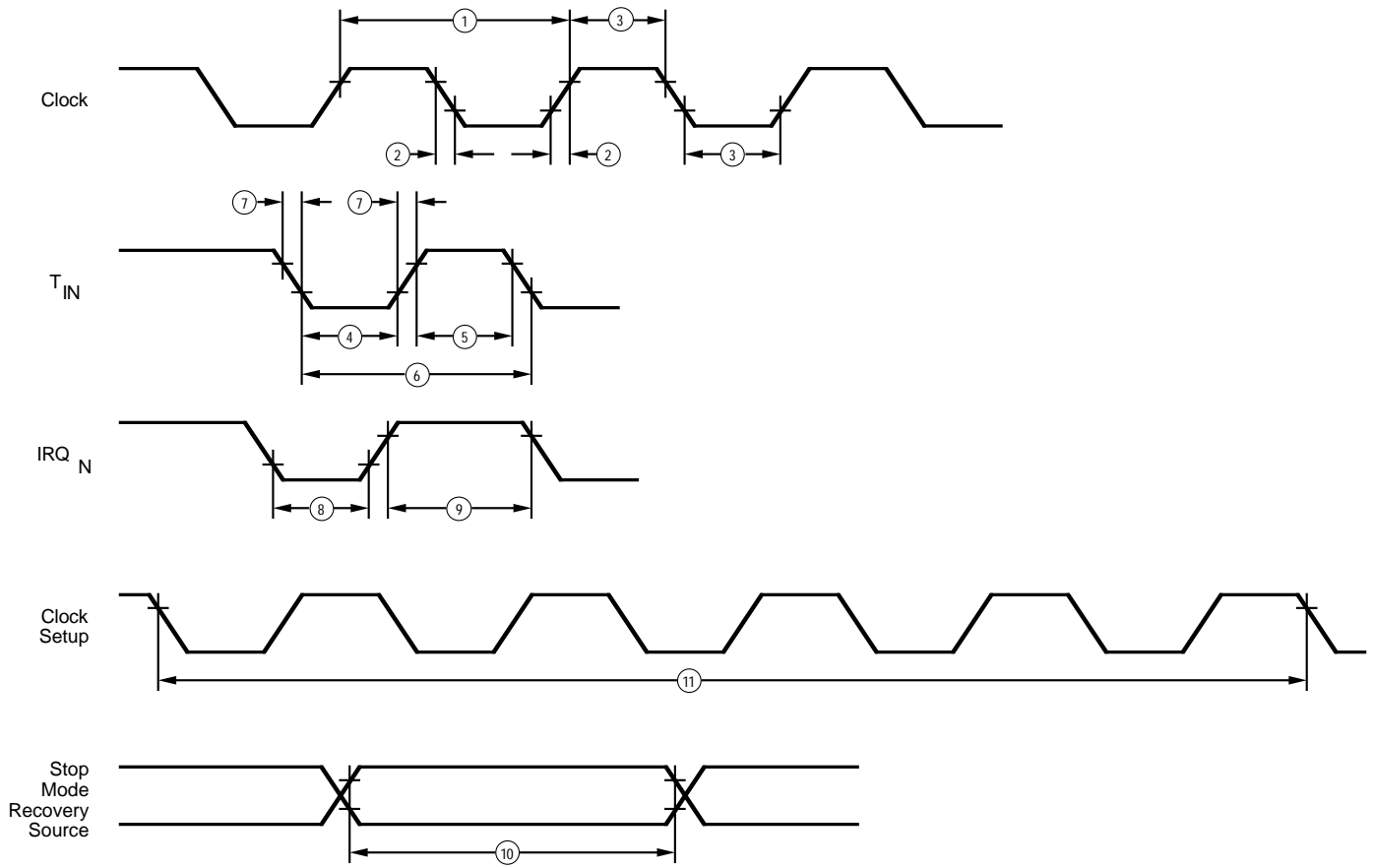
[2] Timing numbers given are for minimum TpC.

[3] 2.0V to 3.9V.

Standard Test Load.

All timing references use 0.9 V<sub>CC</sub> for a logic 1 and 0.1 V<sub>CC</sub> for a logic 0.

**AC CHARACTERISTICS**  
Additional Timing Diagram



**Additional Timing**

**AC CHARACTERISTICS (Z86E73/E74)**

## Additional Timing Table

No	Symbol	Parameter	V <sub>cc</sub> Note [3]	T <sub>A</sub> = 0°C to +70°C 8.0 MHz		Units	Notes	
				Min	Max			
1	TpC	Input Clock Period	4.0V	121	DC	ns	[1]	
			5.5V	121	DC	ns	[1]	
2	TrC,TfC	Clock Input Rise and Fall Times	4.0V		25	ns	[1]	
			5.5V		25	ns	[1]	
3	TwC	Input Clock Width	4.0V	37		ns	[1]	
			5.5V	37		ns	[1]	
4	TwTinL	Timer Input Low Width	4.0V	100		ns	[1]	
			5.5V	70		ns	[1]	
5	TwTinH	Timer Input High Width	4.0V	3TpC			[1]	
			5.5V	3TpC			[1]	
6	TpTin	Timer Input Period	4.0V	8TpC			[1]	
			5.5V	8TpC			[1]	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	4.0V		100	ns	[1]	
			5.5V		100	ns	[1]	
8A	TwIL	Interrupt Request Low Time	4.0V	100		ns	[1, 2]	
			5.5V	70		ns	[1, 2]	
8B	TwIL	Int. Request Low Time	4.0V	3TpC			[1, 3]	
			5.5V	3TpC			[1, 3]	
9	TwIH	Interrupt Request Input High Time	4.0V	3TpC			[1, 2]	
			5.5V	3TpC			[1, 2]	
10	TwsM	Stop-Mode Recovery Width Spec	4.0V	12		ns	[8]	
			5.5V	12		ns	[8]	
			4.0V	5TpC			[7]	
			5.5V	5TpC			[7]	
11	Tost	Oscillator Start-up Time	4.0V		5TpC		[4]	
			5.5V		5TpC		[4]	
12	Twdt	Watch-Dog Timer Delay Time	(5 ms)	4.0V	12	75	ms	D0 = 0 [5]
				5.5V	5	20	ms	D1 = 0 [5]
			(10 ms)	4.0V	25	150	ms	D0 = 1 [5]
				5.5V	10	40	ms	D1 = 0 [5]
			(20 ms)	4.0V	50	300	ms	D0 = 0 [5]
				5.5V	20	80	ms	D1 = 1 [5]
			(80 ms)	4.0V	225	1200	ms	D0 = 1 [5]
				5.5V	80	320	ms	D1 = 1 [5]

**Notes:**

- [1] Timing Reference uses 0.9 V<sub>cc</sub> for a logic 1 and 0.1 V<sub>cc</sub> for a logic 0.
- [2] Interrupt request through Port 3 (P33-P31).
- [3] Interrupt request through Port 3 (P30).
- [4] SMR – D5 = 0.
- [5] Reg. WDTMR.
- [6] 4.0V to 5.5V.
- [7] Reg. SMR – D5 = 0.
- [8] Reg. SMR – D5 = 1.

## AC CHARACTERISTICS (Z86L73/L74)

### Additional Timing Table

No	Symbol	Parameter	V <sub>cc</sub> Note [3]	T <sub>A</sub> = 0°C to +70°C 8.0 MHz		Units	Notes	
				Min	Max			
1	TpC	Input Clock Period	2.0V	121	DC	ns	[1]	
			3.9V	121	DC	ns	[1]	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns	[1]	
			3.9V		25	ns	[1]	
3	TwC	Input Clock Width	2.0V	37		ns	[1]	
			3.9V	37		ns	[1]	
4	TwTinL	Timer Input Low Width	2.0V	100		ns	[1]	
			3.9V	70		ns	[1]	
5	TwTinH	Timer Input High Width	2.0V	3TpC			[1]	
			3.9V	3TpC			[1]	
6	TpTin	Timer Input Period	2.0V	8TpC			[1]	
			3.9V	8TpC			[1]	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0V		100	ns	[1]	
			3.9V		100	ns	[1]	
8A	TwlL	Interrupt Request Low Time	2.0V	100		ns	[1, 2]	
			3.9V	70		ns	[1, 2]	
8B	TwlL	Int. Request Low Time	2.0V	3TpC			[1, 3]	
			3.9V	3TpC			[1, 3]	
9	TwhH	Interrupt Request Input High Time	2.0V	3TpC			[1, 2]	
			3.9V	3TpC			[1, 2]	
10	TwsM	Stop-Mode Recovery Width Spec	2.0V	12		ns	[8]	
			3.9V	12		ns	[8]	
			2.0V	5TpC			[7]	
			3.9V	5TpC			[7]	
11	Tost	Oscillator Start-up Time	2.0V		5TpC		[4]	
			3.9V		5TpC		[4]	
12	Twdt	Watch-Dog Timer Delay Time	(5 ms)	2.0V	12	75	ms	D0 = 0 [5]
				3.9V	5	20	ms	D1 = 0 [5]
			(10 ms)	2.0V	25	150	ms	D0 = 1 [5]
				3.9V	10	40	ms	D1 = 0 [5]
			(20 ms)	2.0V	50	300	ms	D0 = 0 [5]
				3.9V	20	80	ms	D1 = 1 [5]
			(80 ms)	2.0V	225	1200	ms	D0 = 1 [5]
				3.9V	80	320	ms	D1 = 1 [5]

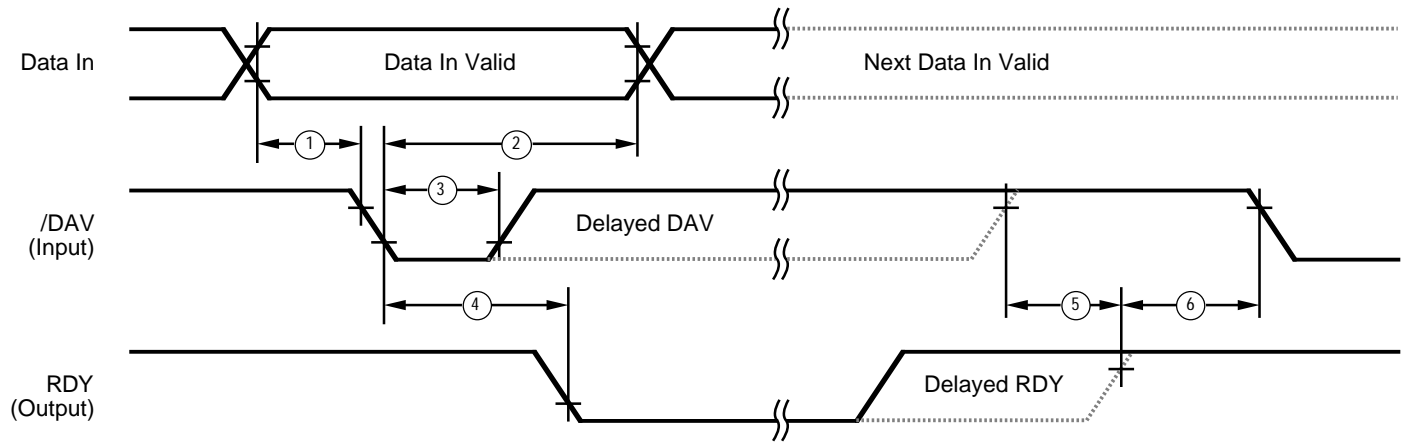
**Notes:**

- [1] Timing Reference uses 0.9 V<sub>cc</sub> for a logic 1 and 0.1 V<sub>cc</sub> for a logic 0.
- [2] Interrupt request through Port 3 (P33-P31).
- [3] Interrupt request through Port 3 (P30).
- [4] SMR – D5 = 0.
- [5] Reg. WDTMR.
- [6] 2.0V to 3.9V.
- [7] Reg. SMR – D5 = 0.
- [8] Reg. SMR – D5 = 1.

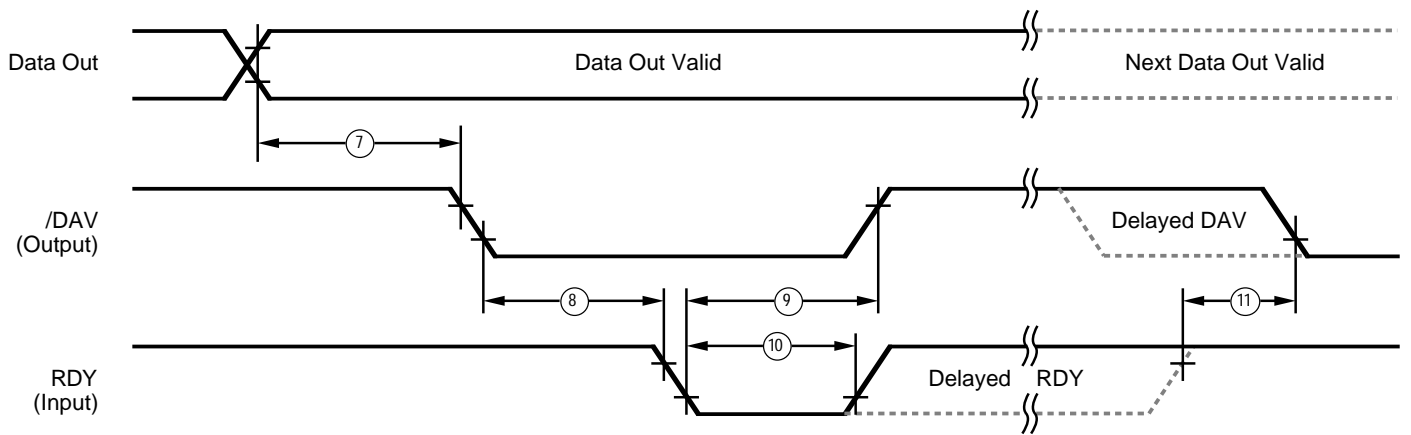


**AC CHARACTERISTICS**

Handshake Timing Diagrams



**Input Handshake Timing**



**Output Handshake Timing**

## AC CHARACTERISTICS (Z86E73/E74)

### Handshake Timing Table

No	Symbol	Parameter	V <sub>cc</sub> Note [3]	T <sub>A</sub> = 0°C to +70°C 8.0 MHz		Data Direction
				Min	Max	
1	TsDI(DAV)	Data In Setup Time	4.0V	0		IN
			5.5V	0		IN
2	ThDI(DAV)	Data In Hold Time	4.0V	160		IN
			5.5V	115		IN
3	TwDAV	Data Available Width	4.0V	155		IN
			5.5V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY Falling Delay	4.0V		160	IN
			5.5V		115	IN
5	TdDAVIId(RDY)	DAV Rising to RDY Falling Delay	4.0V		120	IN
			5.5V		80	IN
6	TdRDY0(DAV)	RDY Rising to DAV Falling Delay	4.0V	0		IN
			5.5V	0		IN
7	TdDO(DAV)	Data Out to DAV Falling Delay	4.0V	63		OUT
			5.5V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY Falling Delay	4.0V	0		OUT
			5.5V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV Rising Delay	4.0V		160	OUT
			5.5V		115	OUT
10	TwRDY	RDY Width	4.0V	110		OUT
			5.5V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV Falling Delay	4.0V		110	OUT
			5.5V		80	OUT

**Note:**

[3] 4.0V to 5.5V.

## AC CHARACTERISTICS (Z86L73/L74)

### Handshake Timing Table

No	Symbol	Parameter	V <sub>cc</sub> Note [3]	T <sub>A</sub> = 0°C to +70°C 8.0 MHz		Data Direction
				Min	Max	
1	TsDI(DAV)	Data In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data In Hold Time	2.0V	160		IN
			3.9V	115		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY Falling Delay	2.0V		160	IN
			3.9V		115	IN
5	TdDAVIId(RDY)	DAV Rising to RDY Falling Delay	2.0V		120	IN
			3.9V		80	IN
6	TdRDY0(DAV)	RDY Rising to DAV Falling Delay	2.0V	0		IN
			3.9V	0		IN
7	TdDO(DAV)	Data Out to DAV Falling Delay	2.0V	63		OUT
			3.9V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY Falling Delay	2.0V	0		OUT
			3.9V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV Rising Delay	2.0V		160	OUT
			3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV Falling Delay	2.0V		110	OUT
			3.9V		80	OUT

**Note:**

[3] 2.0V to 3.9V.