



## Z86L88/L81/L86 INFRARED REMOTE CONTROLLERS

### FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	28-pin DIP, SOIC
Z86L88	16	237	24	X
Z86L81	24	237	24	X
Z86L86	32	237	24	X

\*General-Purpose

- 2.0V to 3.9V Operating Range (8.0 MHz)
- Three Standby Modes (Typical)
  - STOP - 2  $\mu$ A
  - HALT - 0.8 mA
  - Low-Voltage Standby (< VLV)
- Expanded Register File Control Registers
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception

- Five Priority Interrupts
- Low-Voltage Detection and Protection
- Watch-Dog Timer (WDT)/Power-On Reset (POR)
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
  - All Eight Port 2 Bits at One Time or Not
  - Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs
- Maskable 0.4 V<sub>DD</sub> Single Trip Point Inputs on P00 Through P03 for Direct Mouse/Trackball IR Sensor Interface
- Low-Voltage Standby Mode

### GENERAL DESCRIPTION

The Z86L8X family of infrared (IR) consumer controller processors are ROM-based members of the Z8<sup>®</sup> single-chip microcontroller family offering a unique register-to-register architecture that avoids accumulator bottlenecks and offers fast execution of code.

Zilog's CMOS microcontrollers feature fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with low-cost and low-power consumption.

The Z86L8X family architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File (ERF) to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z86L8X offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

**GENERAL DESCRIPTION** (Continued)

For applications demanding powerful I/O capabilities, the Z86L8X fulfills this with two package options in which 24 pins of dedicated input and output are grouped into three ports. Each port consists of eight lines and is configurable under software control to provide timing, status signals, and parallel I/O.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File, and Expanded Register File. (ERF). The Register File is composed of 256 bytes of RAM. It includes four I/O port registers, 15 control and status registers, and the rest are general purpose registers. The ERF consists of two register groups (Banks D and F).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving

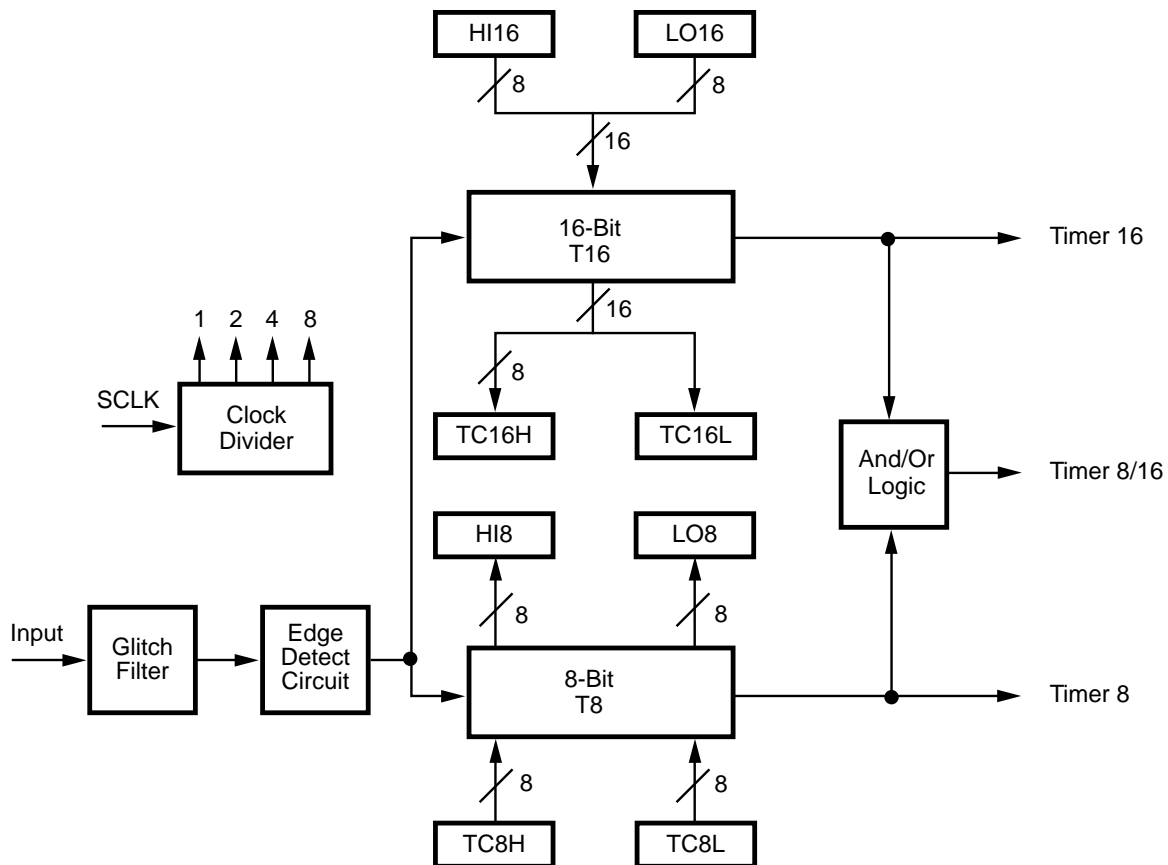
and demodulating complex waveform/pulses, the Z86L8X offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

**Notes:**

All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>



**Figure 1. Counter/Timer Block Diagram**

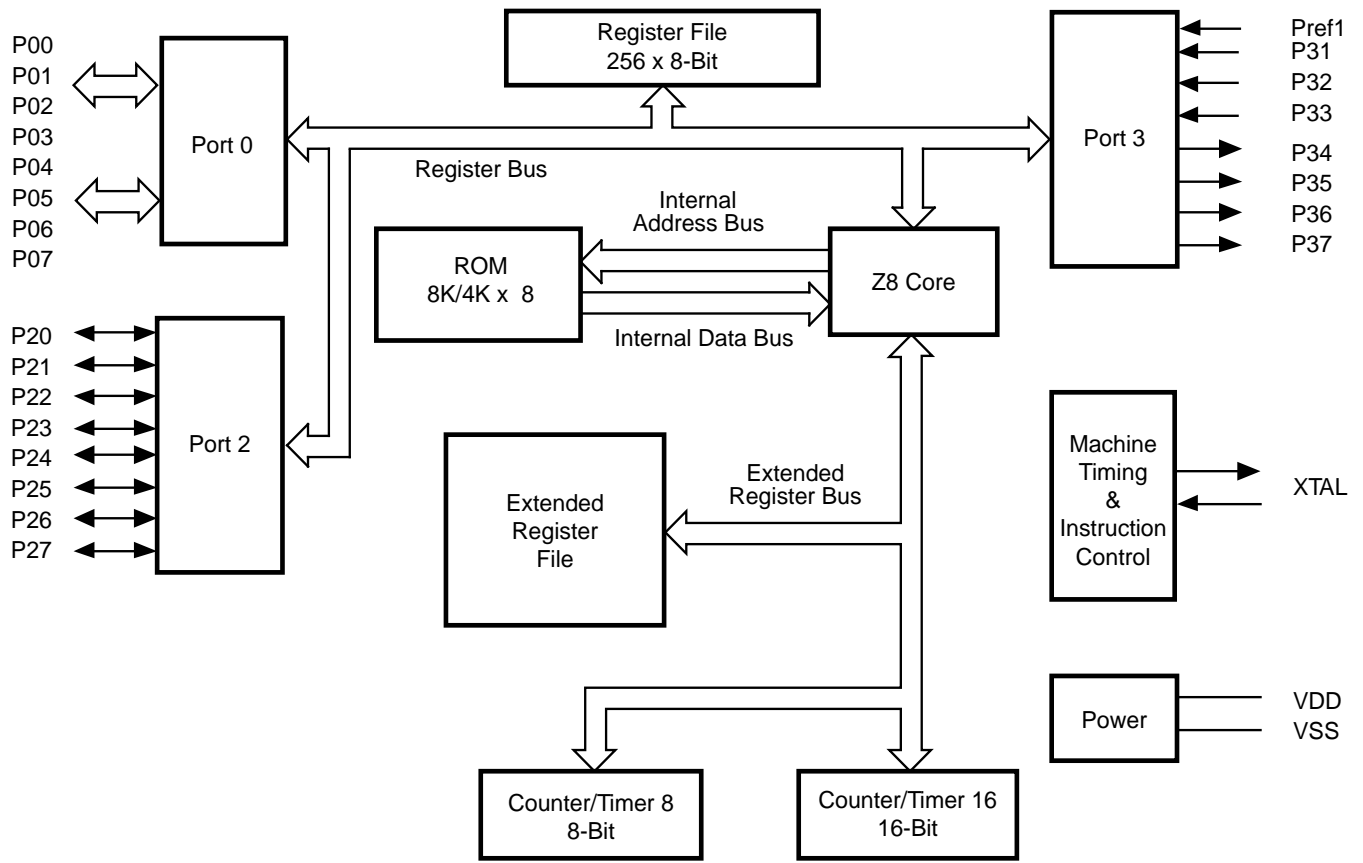


Figure 2. Functional Block Diagram

PIN DESCRIPTION

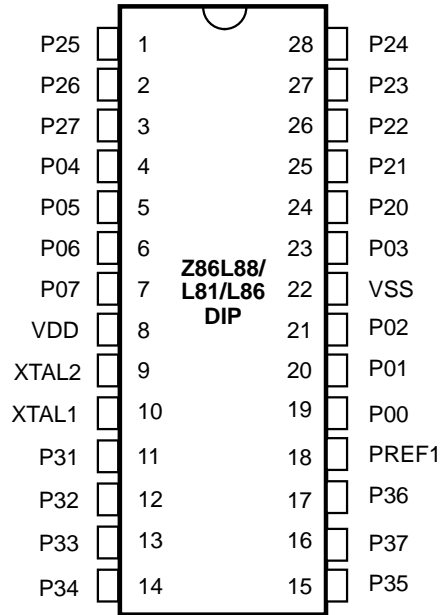


Figure 3. 28-Pin DIP  
Pin Assignments

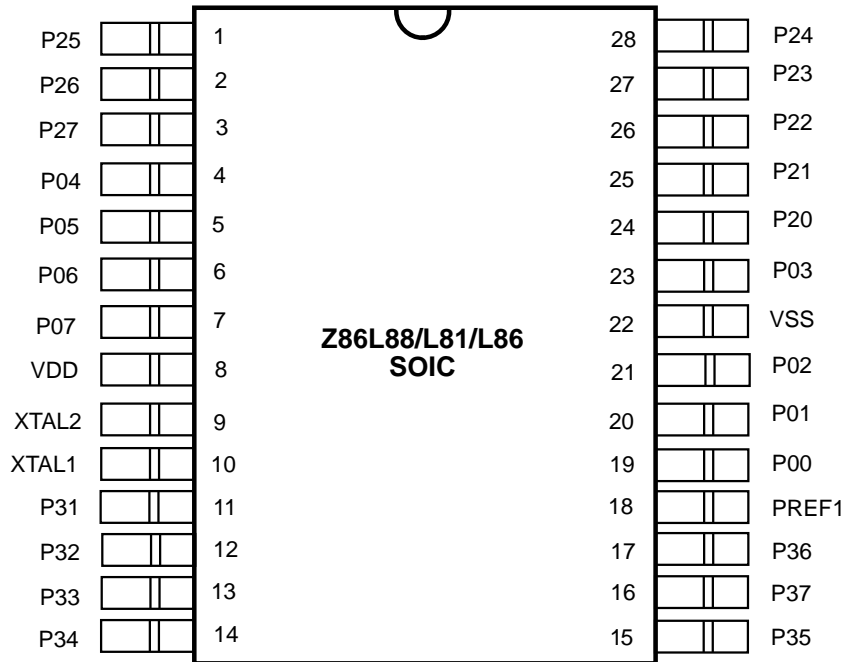


Figure 4. 28-Pin SOIC  
Pin Assignments

**PIN DESCRIPTION** (Continued)

**Table 1. Pin Identification**

28-Pin DIP & SOIC #	Symbol	Direction	Description
1	P25	Input/Output	
2	P26	Input/Output	
3	P27	Input/Output	
4	P04	Input/Output	Port 0 can be configured as a mouse/trackball input.
5	P05	Input/Output	
6	P06	Input/Output	
7	P07	Input/Output	
8	V <sub>DD</sub>		Power Supply
9	XTAL2	Output	Crystal, Oscillator Clock
10	XTAL1	Input	Crystal, Oscillator Clock
11	P31	Input	IRQ2/Modulator Input/Comparator 1 Input
12	P32	Input	IRQ0/Comparator 2 Input
13	P33	Input	IRQ1/Comparator 2 Ref
14	P34	Output	T8 Output
15	P35	Output	T16 Output
16	P37	Output	
17	P36	Output	T8/T16 Output
18	Pref1	Input	Analog Ref Input (Comparator 1)
19	P00	Input/Output	Port 0 is Nibble Programmable.
20	P01	Input/Output	Port 0 can be configured as A15-A8 external program.
21	P02	Input/Output	
22	V <sub>SS</sub>		Ground
23	P03	Output	ROM Address Bus
24	P20	Input/Output	Port 2 pins are individually configurable as input or output.
25	P21	Input/Output	
26	P22	Input/Output	
27	P23	Input/Output	
28	P24	Input/Output	

## ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply Voltage (*)	-0.3	+7.0	V
$T_{STG}$	Storage Temp.	-65°	+150°	C
$T_A$	Oper. Ambient Temp.		†	C

**Notes:**

\* Voltage on all pins with respect to GND.

† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

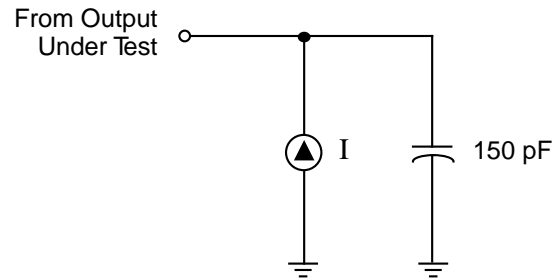


Figure 5. Test Load Diagram

## CAPACITANCE

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$ ,  $f = 1.0 \text{ MHz}$ , unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

**DC CHARACTERISTICS**

Sym	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes [3]
			Min	Max				
V <sub>GH</sub>	Max Input Voltage	20V		7		V	I <sub>IN</sub> < 250µA	
		39V		7		V	I <sub>IN</sub> < 250µA	
	Clock Input High Voltage	20V	0.9V <sub>CC</sub>	V <sub>CC</sub> +0.3		V	Driven by External Clock Generator	
		39V	0.9V <sub>CC</sub>	V <sub>CC</sub> +0.3		V	Driven by External Clock Generator	
V <sub>GL</sub>	Clock Input Low Voltage	20V	V <sub>SS</sub> -0.3	0.2V <sub>CC</sub>		V	Driven by External Clock Generator	
		39V	V <sub>SS</sub> -0.3	0.2V <sub>CC</sub>		V	Driven by External Clock Generator	
V <sub>H</sub>	Input High Voltage	20V	0.7V <sub>CC</sub>	V <sub>CC</sub> +0.3	1.3	V		
		39V	0.7V <sub>CC</sub>	V <sub>CC</sub> +0.3	2.5	V		
V <sub>L</sub>	Input Low Voltage	20V	V <sub>SS</sub> -0.3	0.2V <sub>CC</sub>	0.5	V		
		39V	V <sub>SS</sub> -0.3	0.2V <sub>CC</sub>	0.9	V		
V <sub>GH1</sub>	Output High Voltage	20V	V <sub>CC</sub> -0.4		1.7	V	I <sub>OH</sub> = -0.5mA	†
		39V	V <sub>CC</sub> -0.4		3.7	V	I <sub>OH</sub> = -0.5mA	
V <sub>GH2</sub>	Output High Voltage (P36, P37)	20V	V <sub>CC</sub> -0.7		1.5	V	I <sub>OH</sub> = -7mA	[10]
		39V	V <sub>CC</sub> -0.7		3.5	V	I <sub>OH</sub> = -7mA	[10]
V <sub>OL1</sub>	Output Low Voltage	20V		0.4	0.1	V	I <sub>OL</sub> = 1.0mA	*
		39V		0.4	0.2	V	I <sub>OL</sub> = 4.0mA	
V <sub>OL2</sub>	Output Low Voltage	20V		0.8	0.6	V	I <sub>OL</sub> = 5.0mA	*
		39V		0.8	0.3	V	I <sub>OL</sub> = 7.0mA	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	20V		0.8	0.3	V	I <sub>OL</sub> = 10mA	[9]
		39V		0.8	0.2	V	I <sub>OL</sub> = 10mA	[9]
V <sub>GHSET</sub>	Comparator Input Offset Voltage	20V		25	10	mV		
		39V		25	10	mV		
I <sub>L</sub>	Input Leakage	20V	-1	1	<1	µA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		39V	-1	1	<1	µA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>L</sub>	Output Leakage	20V	-1	1	<1	µA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
		39V	-1	1	<1	µA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>R</sub>	Reset Input Current	20V		-45	-20	µA		
I <sub>CC</sub>	Supply Current	39V		-55	-30	µA		
		20V		10	4	nA	@ 8.0MHz	[4, 5]
		39V		15	10	nA	@ 8.0MHz	[4, 5]
		20V		100	10	µA	@ 32kHz	[4, 5, 11]
	39V		300	10	µA	@ 32kHz	[4, 5, 11]	

**DC CHARACTERISTICS** (Continued)

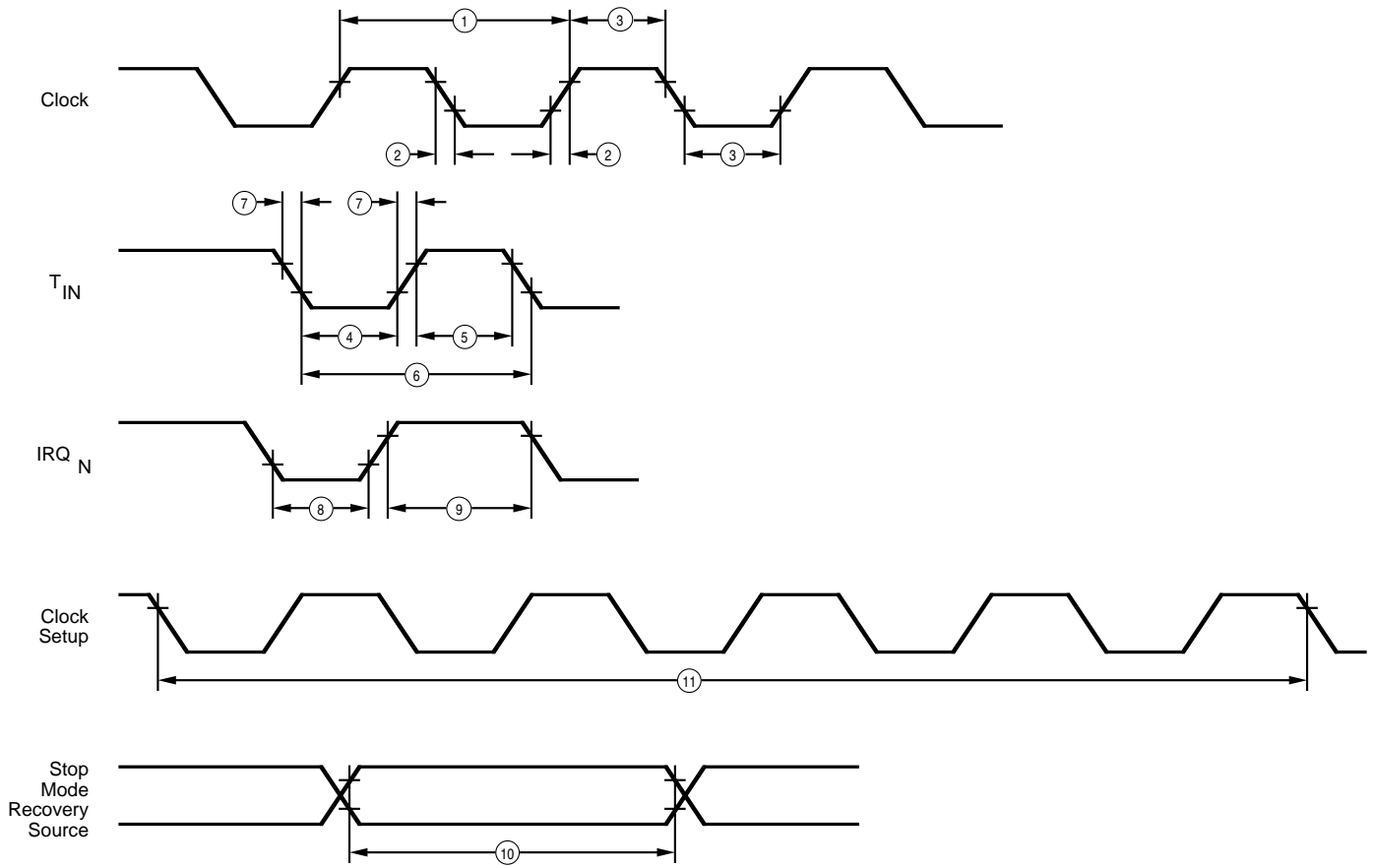
Sym	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 0°C to +70°C		Typ @ 25°C	Units	Conditions	Notes [3]
			Min	Max				
I <sub>CC1</sub>	Standby Current (WDTOff)	20V		3	1	nA	HALTMode V <sub>IN</sub> =0V, V <sub>CC</sub> @ 8.0MHz	[4,5]
		39V		5	4	nA	HALTMode V <sub>IN</sub> =0V, V <sub>CC</sub> @ 8.0MHz	[4,5]
	20V		2	0.8	nA	ClockDivide-by-16 @ 8.0MHz	[4,5]	
	39V		4	2.5	nA	ClockDivide-by-16 @ 8.0MHz	[4,5]	
I <sub>CC2</sub>	Standby Current	20V		8	2	µA	STOPMode V <sub>IN</sub> =0V, V <sub>CC</sub> WDTisnotRunning	[6,8]
		39V		10	3	µA	STOPMode V <sub>IN</sub> =0V, V <sub>CC</sub> WDTisnotRunning	[6,8]
	20V		500	310	µA	STOPMode V <sub>IN</sub> =0V, V <sub>CC</sub> WDTisRunning	[6,8]	
	39V		800	600	µA	STOPMode V <sub>IN</sub> =0V, V <sub>CC</sub> WDTisRunning	[6,8]	
T <sub>TR</sub>	Power-OnReset	20V	7.5	75	13	ms		
		39V	2.5	20	7	ms		
V <sub>LV</sub>	V <sub>CC</sub> Low Voltage Protection			2.15	1.7	V	8MHzmax Ext.CLKFreq.	[7]

**Notes:**

- | [1] | I <sub>CC1</sub>     | Typ    | Max | Unit | Frequency |
|-----|----------------------|--------|-----|------|-----------|
|     | Crystal/Resonator    | 4.0 mA | 5   | mA   | 8.0 MHz   |
|     | External Clock Drive | 0.3 mA | 5   | mA   | 8.0 MHz   |
- [2] GND = 0V  
 [3] 2.0V to 3.9V  
 [4] All outputs unloaded, I/O pins floating, inputs at rail.  
 [5] CL1 = CL2 = 100 pF  
 [6] Same as note [4] except inputs at V<sub>CC</sub>.  
 [7] The V<sub>LV</sub> increases as the temperature decreases.  
 [8] Oscillator stopped.  
 [9] Two outputs at a time, independent to other outputs.  
 [10] One at a time.  
 [11] 32 kHz clock driver input.
- † All outputs excluding P36, P37.  
 \* All outputs excluding P36, P37, P00, and P01.



**AC CHARACTERISTICS**  
Additional Timing Diagram



**Figure 6. Additional Timing**

**AC CHARACTERISTICS**

## Additional Timing Table

No	Symbol	Parameter	V <sub>cc</sub> Note [3]	T <sub>A</sub> = 0°C to +70°C 8.0MHz		Units	Notes
				Min	Max		
1	TpC	InputClockPeriod	20V	121	DC	ns	[1]
			39V	121	DC	ns	[1]
2	TiC,TfC	ClockInputRise andFallTimes	20V		25	ns	[1]
			39V		25	ns	[1]
3	TwC	InputClockWidth	20V	37		ns	[1]
			39V	37		ns	[1]
4	TwTnL	TimerInput LowWidth	20V	100		ns	[1]
			39V	70		ns	[1]
5	TwTnH	TimerInput HighWidth	20V	3TpC			[1]
			39V	3TpC			[1]
6	TpTin	TimerInputPeriod	20V	8TpC			[1]
			39V	8TpC			[1]
7	TfTin,TfTin	TimerInputRise andFallTimers	20V		100	ns	[1]
			39V		100	ns	[1]
8A	TwL	InterruptRequest LowTime	20V	100		ns	[1,2]
			39V	70		ns	[1,2]
8B	TwL	Int. Request LowTime	20V	3TpC			[1,3]
			39V	3TpC			[1,3]
9	TwH	InterruptRequest InputHighTime	20V	3TpC			[1,2]
			39V	3TpC			[1,2]
10	Twsn	Stop-ModeRecovery WidthSpec	20V	12		ns	[8]
			39V	12		ns	[8]
			20V	5TpC			[7]
			39V	5TpC			[7]
11	Tost	Oscillator Start-upTime	20V		5TpC		[4]
			39V		5TpC		[4]
12	Twdt	Watch-DogTimer (5ms) DelayTime	20V	12	75	ms	D0=0[5]
			39V	5	20	ms	D1=0[5]
			20V	25	150	ms	D0=1[5]
			39V	10	40	ms	D1=0[5]
			20V	50	300	ms	D0=0[5]
			39V	25	80	ms	D1=1[5]
			20V	225	1200	ms	D0=1[5]
			39V	100	320	ms	D1=1[5]

**Notes:**

- [1] Timing Reference uses 0.9 V<sub>cc</sub> for a logic 1 and 0.1 V<sub>cc</sub> for a logic 0.
- [2] Interrupt request through Port 3 (P33-P31).
- [3] Interrupt request through Port 3 (P30).
- [4] SMR – D5 = 0
- [5] Reg. WDTMR
- [6] 2.0V to 3.9V
- [7] Reg. SMR – D5 = 0
- [8] Reg. SMR – D5 = 1

---

© 1996 by Zilog, Inc. All rights reserved. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Zilog, Inc. The information in this document is subject to change without notice. Devices sold by Zilog, Inc. are covered by warranty and patent indemnification provisions appearing in Zilog, Inc. Terms and Conditions of Sale only. Zilog, Inc. makes no warranty, express, statutory, implied or by description, regarding the information set forth herein or regarding the freedom of the described devices from intellectual property infringement. Zilog, Inc. makes no warranty of merchantability or fitness for any purpose. Zilog, Inc. shall not be responsible for any errors that may appear in this document. Zilog, Inc. makes no commitment to update or keep current the information contained in this document.

Zilog's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the customer and Zilog prior to use. Life support devices or systems are those which are intended for surgical implantation into the body, or which sustains life whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

Zilog, Inc. 210 East Hacienda Ave.  
Campbell, CA 95008-6600  
Telephone (408) 370-8000  
FAX 408 370-8056  
Internet: <http://www.zilog.com>