PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86C63/64

CMOS Z8®
32K ROM MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C63/64 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C63/64 is a member of the Z8 single-chip microcontroller family with 32 Kbytes of ROM and 256 bytes of RAM.

The Z86C63 is housed in a 40-pin DIP, and a 44-pin PLCC package, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin version only. The Z86C64 is housed in a 64-pin DIP, and a 68-pin PLCC. Both versions of the Z86C64 have the ROMless pin option, which allows both external memory and preprogrammed ROM, enabling this Z8 microcontroller to be used in high-volume applications or where code flexibility is required. The Z86C96 ROMless Z8 will support the Z86C63/64.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C63/64 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C63 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. The Z86C64 has 52 pins for input and output, and these lines are grouped into six, 8-bit ports and one 4-bit port. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

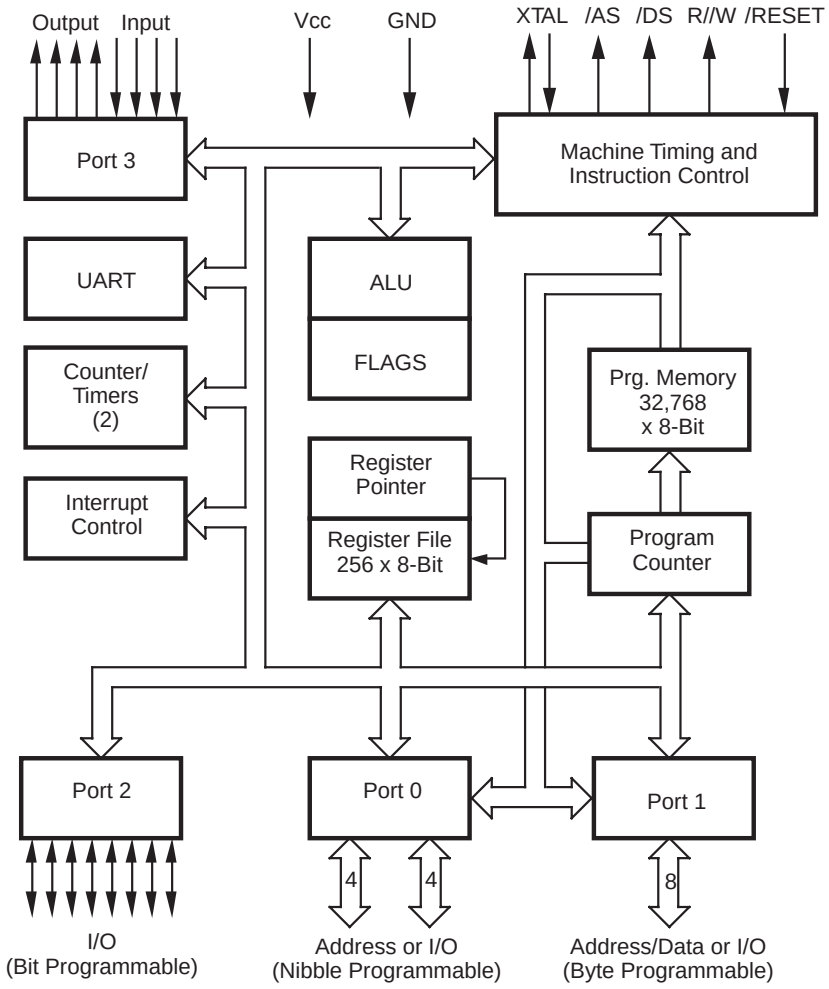
To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C63/64 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Block Diagrams).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

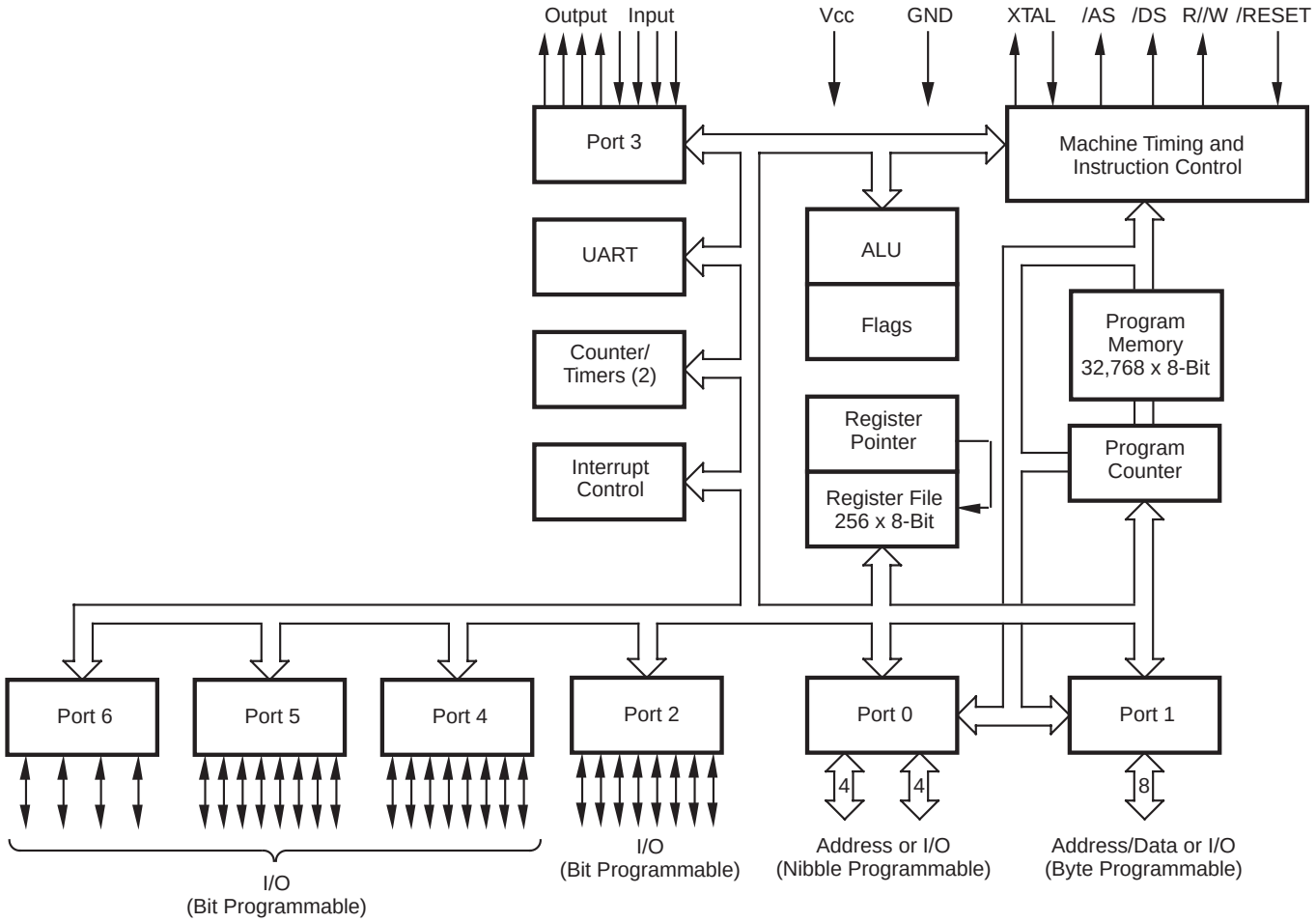
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION

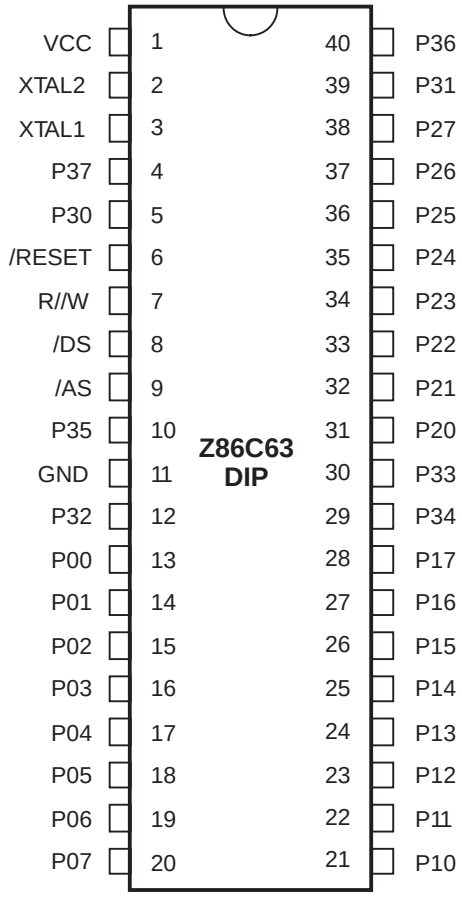


Z86C63 Functional Block Diagram



Z86C64 Functional Block Diagram

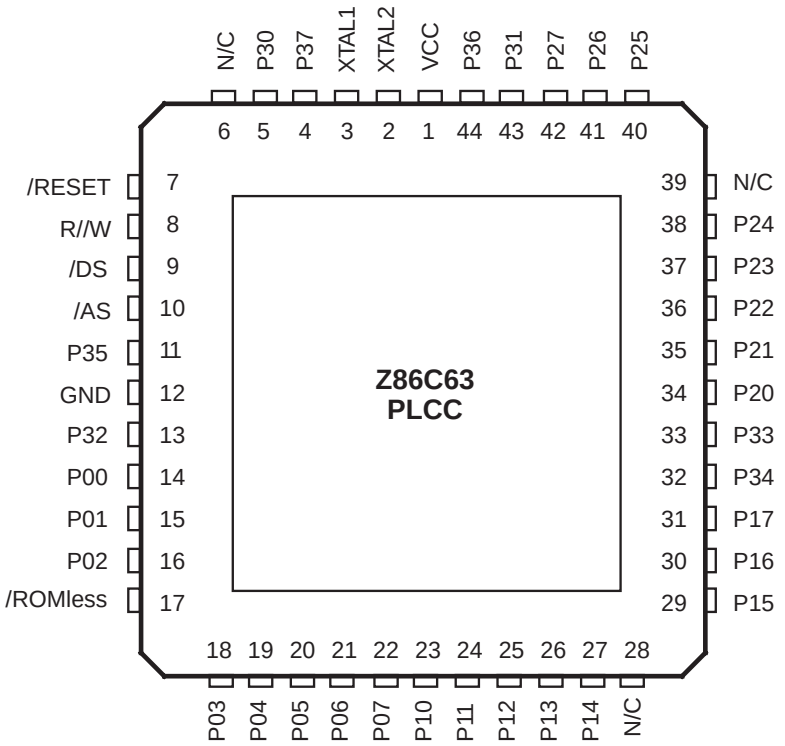
PIN DESCRIPTION



Z86C63 40-Pin DIP
Pin Assignments

Z86C63 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R//W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

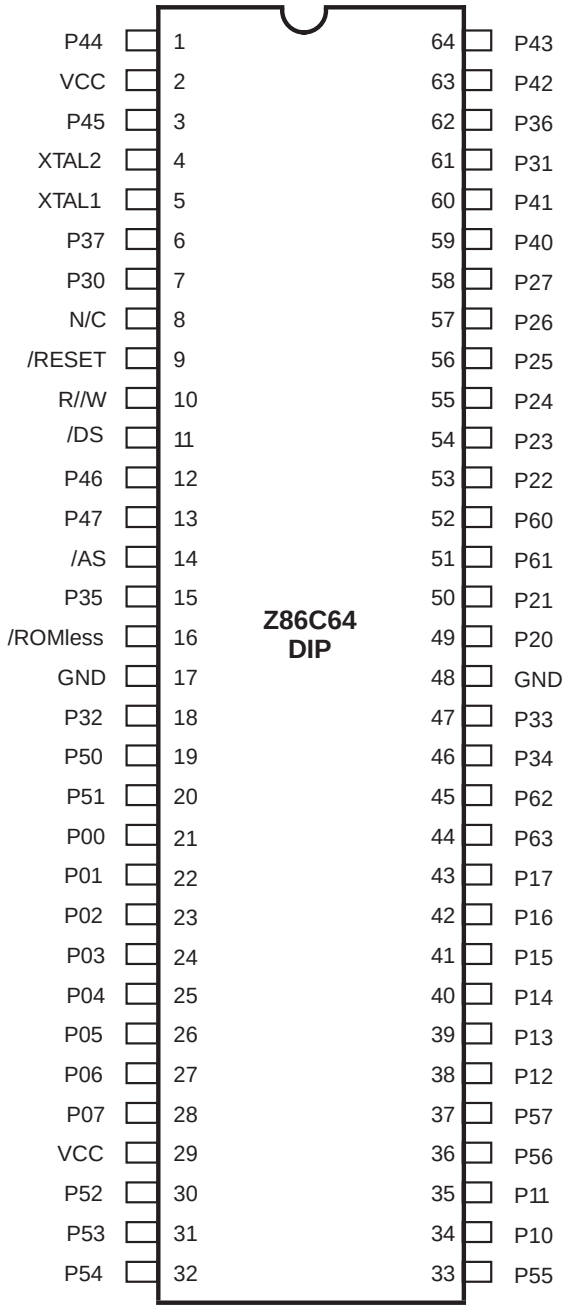


Z86C63 44-Pin PLCC Pin Assignments

Z86C63 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8	R//W	Read/Write	Output
9	/DS	Data Strobe	Output
10	/AS	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02-P00	Port 0, Pins 0,1,2	In/Output
17	/ROMless	ROM/ROMless control	Input
18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output
23-27	P14-P10	Port 1, Pins 0,1,2,3,4	In/Output
28	N/C	Not Connected	Input
29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
39	N/C	Not Connected	Input
40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

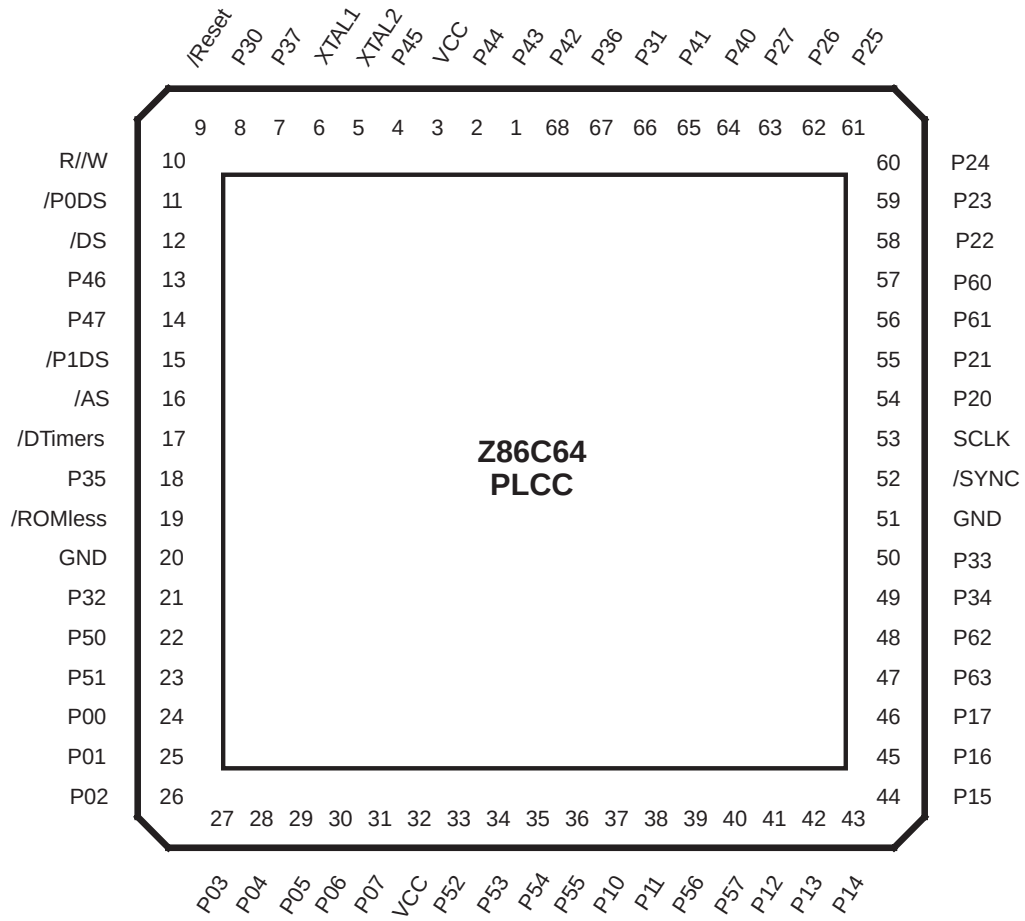
PIN DESCRIPTION (Continued)



Z86C64 64-Pin DIP Pin Assignments

Z86C64 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V_{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	/ROMless	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V_{CC}	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output



Z86C64 68-Pin PLCC Pin Assignments

PIN DESCRIPTION (Continued)

Z86C64 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output
3	V_{CC}	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output
6	XTAL1	Crystal, Oscillator Clock	Input
7	P37	Port 3, Pin 7	Output
8	P30	Port 3, Pin 0	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/P0DS	Port 0 Data Strobe	Output
12	/DS	Data Strobe	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output
15	/P1DS	Port 1, Data Strobe	Output
16	/AS	Address Strobe	Output
17	/DTIMER	DTIMER	Input
18	P35	Port 3, Pin 5	Output
19	/ROMless	ROM/ROMless control	Input
20	GND	Ground	Input
21	P32	Port 3, Pin 2	Input
22-23	P51-P50	Port 5, Pins 0,1	In/Output
24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
32	V_{CC}	Power Supply	Input
33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
37-38	P11-P10	Port 1, Pins 0,1	In/Output
39-40	P56-P57	Port 5, Pins 6,7	In/Output
41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
47-48	P63-P62	Port 6, Pins 3,2	In/Output
49	P34	Port 3, Pin 4	Output
50	P33	Port 3, Pin 3	Input
51	GND	Ground	Input
52	/SYNC	Synchronization	Output
53	SCLK	System Clock	Output
54-55	P21-P20	Port 2, Pins 0,1	In/Output
56-57	P60-P61	Port 6, Pins 1,0	In/Output
58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
64-65	P41-P40	Port 4, Pins 0,1	In/Output
66	P31	Port 3, Pin 1	Input
67	P36	Port 3, Pin 6	Output
68	P42	Port 4, Pin 2	In/Output

ABSOLUTE MAXIMUM RATINGS

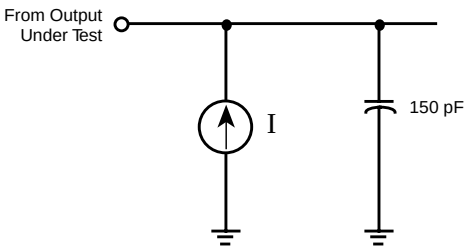
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
* Voltages on all pins with respect to GND.
† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).



Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Z86C63

Sym	Parameter	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	[4] I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS} – 0.3	0.8	V_{SS} – 0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC} + 0.3	2	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	V_{SS} – 0.3	0.2 V_{CC}	V_{SS} – 0.3	0.2 V_{CC}		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage		V_{CC} – 100 mV		V_{CC} – 100 mV		V	I_{OH} = –100 µA
V_{OH}	Output High Voltage (Low EMI)	2.4		2.4			V	I_{OH} = –0.5 mA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA [3]
V_{OL}	Output Low Voltage (Low EMI)		0.4		0.4		V	I_{OL} = +2.0 mA [3]
V_{OL}	Output Low Voltage		0.6		0.6		V	I_{OL} = +4.0 mA [2]
V_{OL}	Output Low Voltage (Low EMI)		0.6		0.6		V	I_{OL} = +1.0 mA [2]
V_{RH}	Reset Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2 V_{CC}	–0.3	0.2 V_{CC}		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{IR}	Reset Input Current		–180		–180		µA	V_{RL} = 0 V
I_{CC}	Supply Current (Standard Mode)		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current (Standard Mode)		40		40	30	mA	[1] @ 20 MHz
I_{CC}	Supply Current (Low EMI)		6.0			4.0	mA	@ 4 MHz
I_{CC1}	Standby Current (Standard Mode)		15		15	4.5	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC1}	Standby Current (Low EMI)		1.6			0.8	mA	@ 4 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1] STOP Mode V_{IN} = 0 V, V_{CC}
I_{ALL}	Auto Latch Low Current	–14	14	–20	20	5	µA	

Notes:

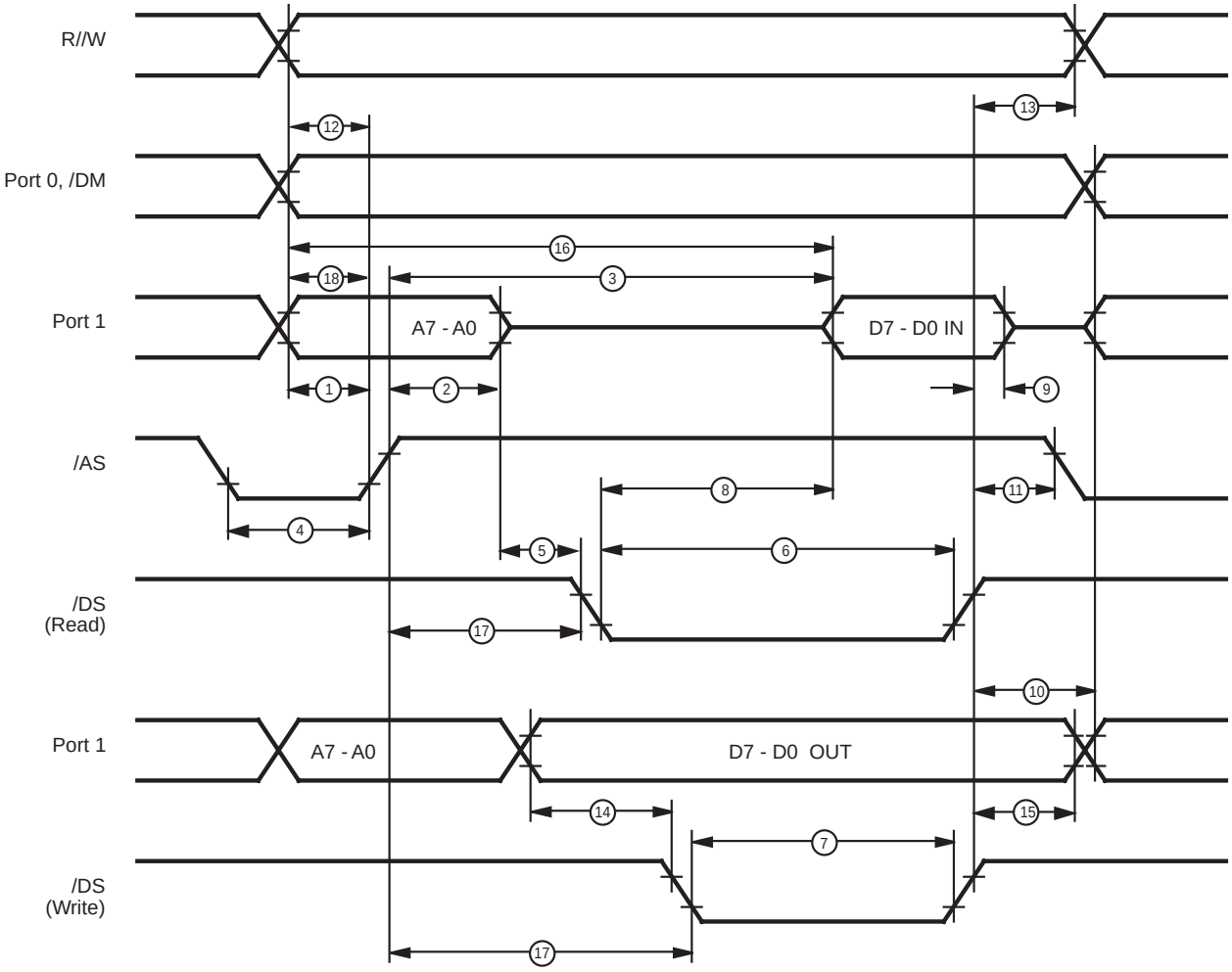
[1] All inputs driven to either 0V or V_{CC}, outputs floating.

[2] V_{CC} = 3.0V to 3.6V

[3] V_{CC} = 4.5V to 5.5V

[4] /Reset pin must be a maximum of V_{CC} + 0.3V.

AC CHARACTERISTICS



External I/O or Memory Read/Write

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C63/64 (16 MHz—Standard Mode Only[4])

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	T_A = –40°C to +105°C 16 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	[1,2,3]
4	TwAS	/AS Low Width	40		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	80		80		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	25		25		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	35		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] Low EMI is not selected.

Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS

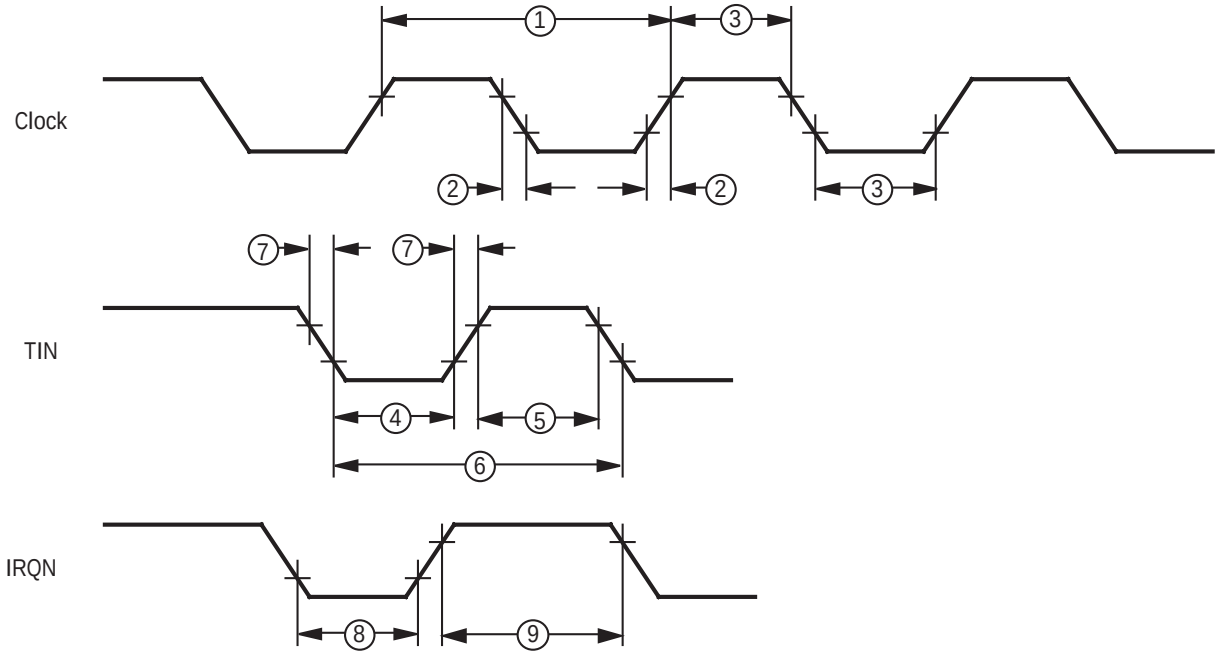
External I/O or Memory Read and Write Timing
Z86C63/64 (20 MHz—Standard Mode Only[4])

No	Symbol	Parameter	T_A = 0°C to +70°C 20 MHz Min	Max	T_A = –40°C to +105°C 20 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	[1,2,3]
4	TwAS	/AS Low Width	30		30		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	65		65		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS rise Delay	20		20		ns	[2,3]
13	TdDS(R/W)	/DS rise to R//W Not Valid	25		25		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] Low EMI is not selected.

Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

AC CHARACTERISTICS
Additional Timing Diagram



Additional Timing

AC CHARACTERISTICS
Additional Timing Table
Z86C63 (Standard Mode Only)

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		10	ns	[1]
3	TwC	Input Clock Width	25/31		25/31		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	[2,3]

Notes:
[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS

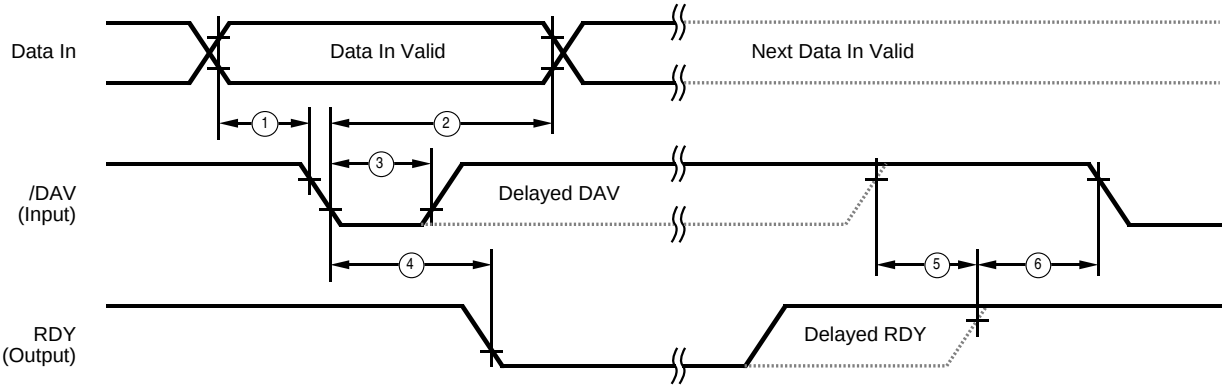
Additional Timing Table
Z86C63 (Low EMI Mode Only)

No	Symbol	Parameter	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = –40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	250	DC	250	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		10	ns	[1]
3	TwC	Input Clock Width	125		125		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	3 TpC		3 TpC		ns	[2]
6	TpTin	Timer Input Period	4 TpC		4 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	3 TpC		3 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	3 TpC		3 TpC		ns	[2,3]

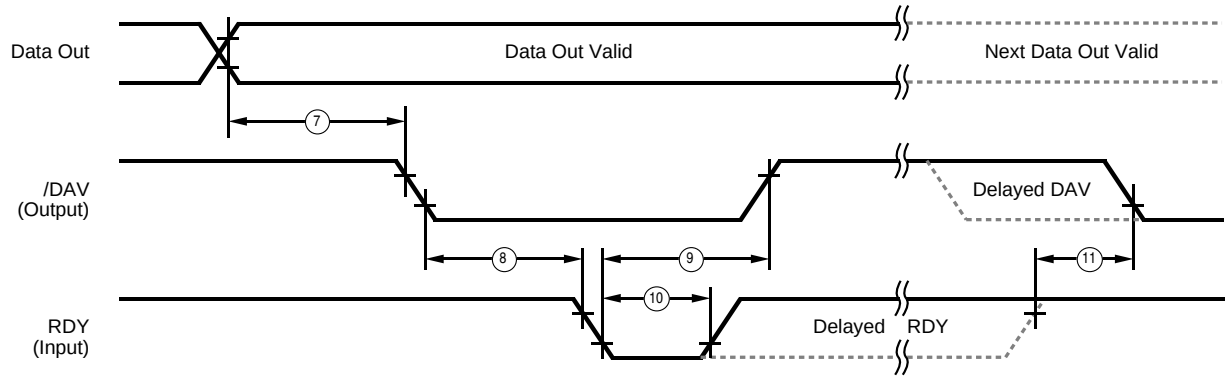
Notes:
[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table
Z86C63

No	Symbol	Parameter	T_A = 0°C to +70°C 20/16 MHz Min	Max	T_A = –40°C to +105°C 20/16 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	115		115		IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV Fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	115		115		OUT

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