Z86C90/C89
ROMLESS CMOS Z8® 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C90/C89 CCP™ (Consumer Controller Processor) introduces a new level of sophistication to single-chip architecture. The Z86C90/C89 are ROMless members of the Z8 single-chip microcontroller family with 236 bytes of general purpose RAM. The only difference that exists between the Z86C89 and the Z86C90 is that the on-chip oscillator of the Z86C89 can accept an external RC network or other external clock source, while the Z86C90's on-chip oscillator accepts a crystal, ceramic resonator, LC, or external clock source drive. The CCP controllers are housed in a 40-pin DIP, 44-pin Leaded Chip Carrier, or a 44-pin Quad Flat Pack, and are CMOS compatible. The CCP offers the use of external memory which enables this Z8 microcomputer to be used where code flexibility is required. Zilog's CMOS microcomputer offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C90/C89 architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, automotive, computer peripherals, and advanced scientific applications.

The CCP applications demand powerful I/O capabilities. The Z86C90/C89 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are four basic address spaces available to support this wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Register File is composed of 236 bytes of general purpose registers, four I/O port registers, and fifteen control and status registers. The Expanded Register File consists of two control registers.

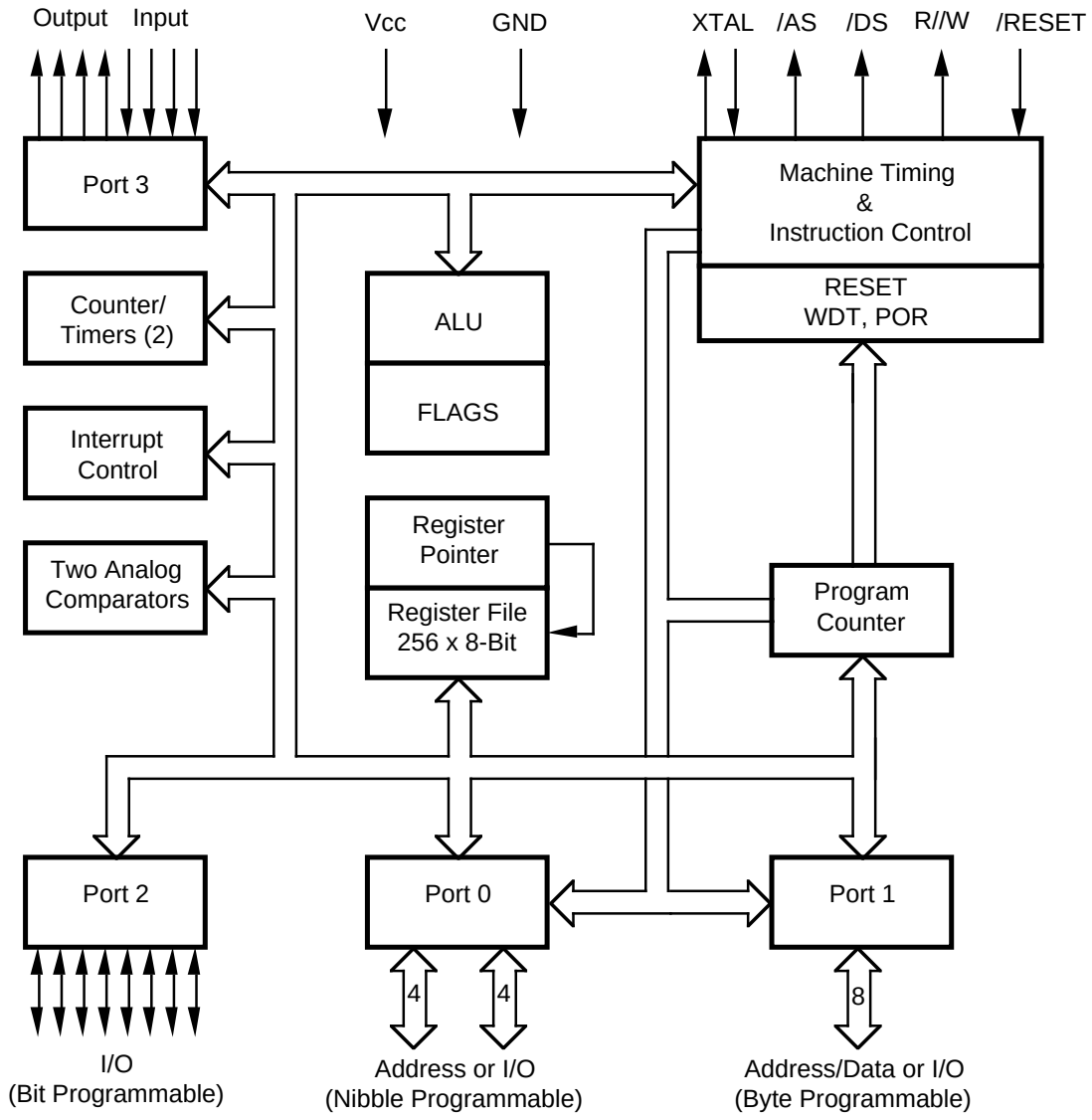
To unburden the program from coping with the real-time problems, such as counting/timing and data communication, the Z86C90/C89 offers two on-chip counter/timers. Included are a large number of user selectable modes, and two on-board comparators to process analog signals with a common reference voltage (see Functional Block Diagram).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

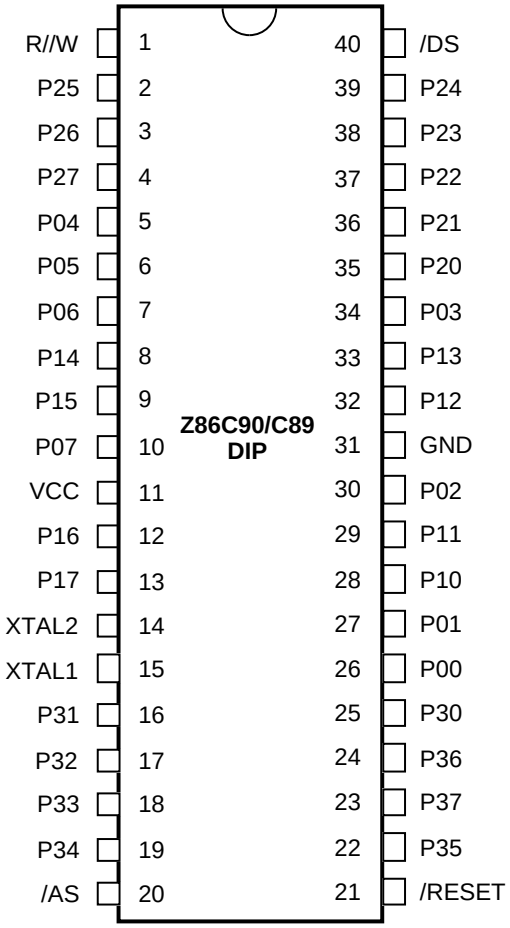
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



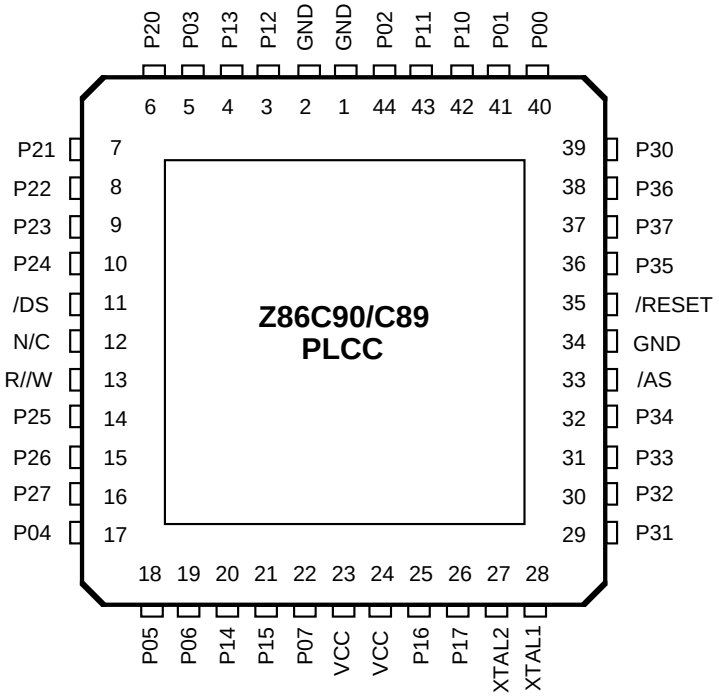
Functional Block Diagram

PIN DESCRIPTION

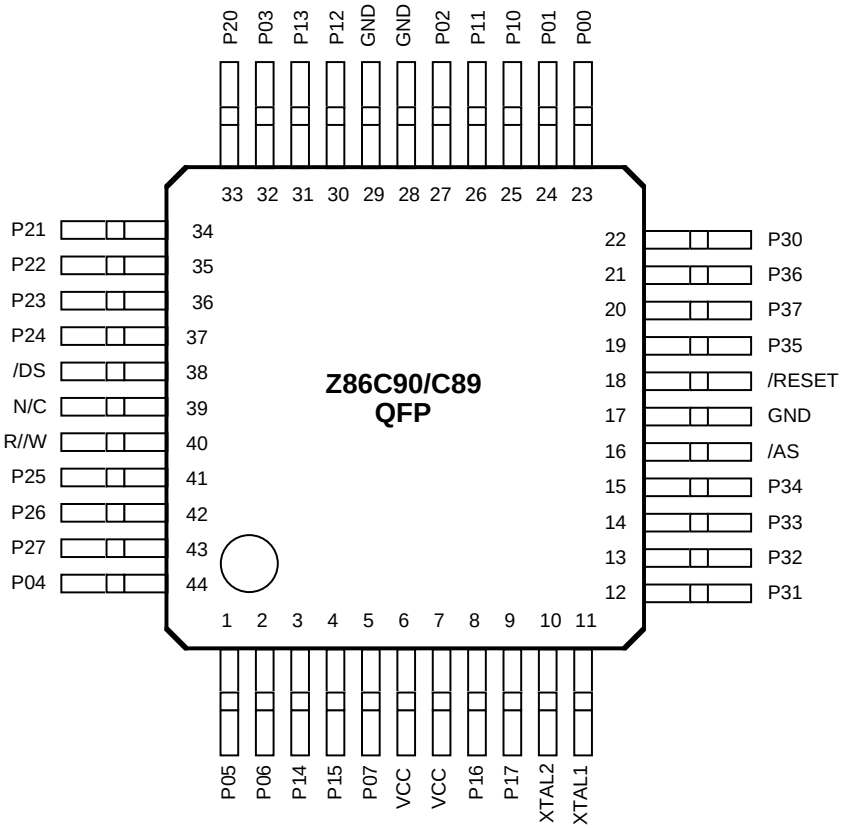


40-Pin DIP Pin Assignments

PIN DESCRIPTION (Continued)



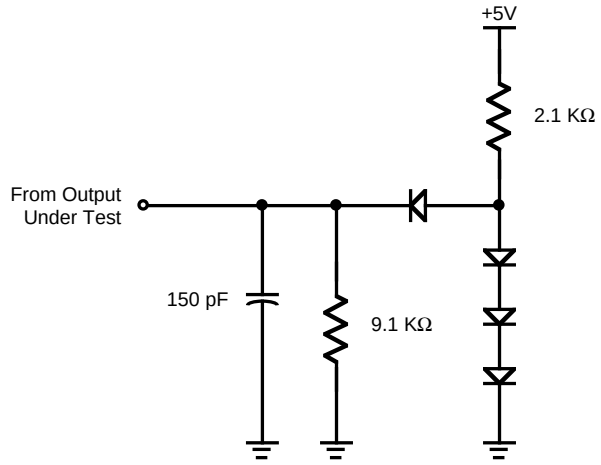
44-Pin PLCC Pin Assignments



44-Pin QFP Pin Assignments

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes: * Voltage on all pins with respect to GND.
† See Ordering Information.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins to GND

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

PLEASE NOTE

These devices will not operate in extended timing mode. Set Register 248, D5 = 0.

DC CHARACTERISTICS

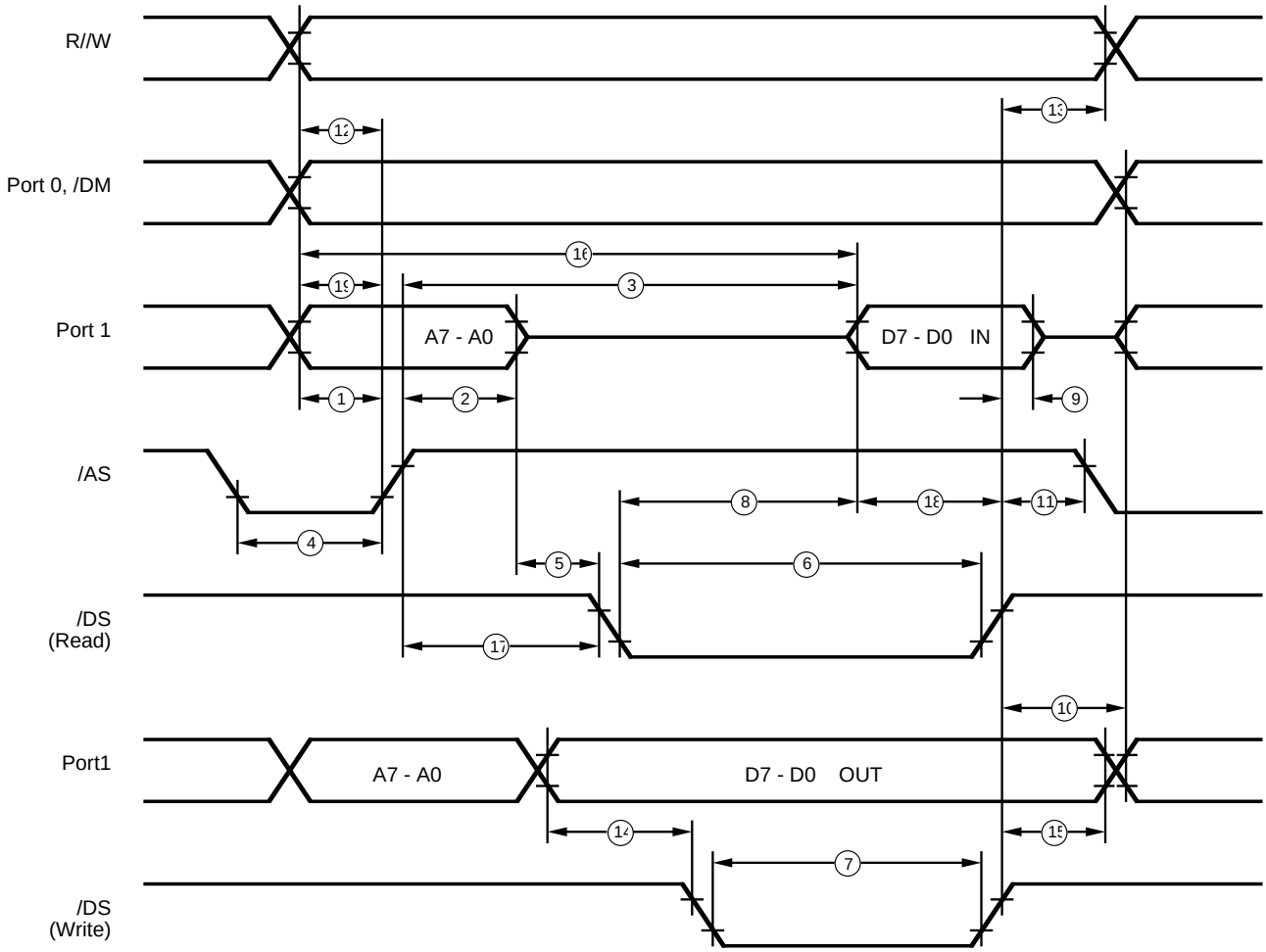
Sym Notes	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	Max	T_A = -40° C to 105° C Min	Max	Typ @ 25°C	Units	Conditions
	Max Input Voltage	3.3V		7		7		V	I_{IN} 250µA
		5.0V		7		7		V	I_{IN} 250µA
V_{CH}	Clock Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.3V	GND -0.30.2 V_{CC}		GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator
		5.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	
V_{IL}	Input Low Voltage	3.3V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	
		5.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltge	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OH} = -2.0 mA
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA
V_{OL1}	Output Low Voltage	3.3V		0.6		0.6	0.2	V	I_{OH} = +4.0 mA
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA
V_{OL2}	Output Low Voltage	3.3V		1.2		1.2	0.3	V	I_{OL} = +6 mA, 3 Pin Max
		5.0V		1.2		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max
V_{RH}	Reset Input	3.3V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V	
	High Voltage	5.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V	
V_{Rl}	Reset Input	3.3V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1		
	Low Voltage	5.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7		
V_{OFFSET}	Comparator Input	3.3V		25		25	10	mV	
	Offset Voltage	5.0V		25		25	10	mV	
I_{IL}	Input Leakage	3.3V	-1	1	-1	2	< 1	µA	V_{IN} = OV, V_{CC}
		5.0V	-1	1	-1	2	< 1	µA	V_{IN} = OV, V_{CC}
I_{OL}	Output Leakage	3.3V	-1	1	-1	2	< 1	µA	V_{IN} = OV, V_{CC}
		5.0V	-1	1	-1	2	< 1	µA	V_{IN} = OV, V_{CC}
I_{IR}	Reset Input Current	3.3V		-45		-60	-20	µA	
		5.0V		-55		-70	-30	µA	
I_{CC} [4,5]	Supply Current	3.3V		10		10	4	mA	@ 8 MHz
		5.0V		15		15	10	mA	@ 8 MHz
[4,5]		3.3V		15		15	5	mA	@ 12 MHz

[4,5]							
		5.0V		20	20	15	mA @ 12 MHz
[4,5]							

Sym Notes	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	Max	T_A = -40° C to 105° C Min	Max	Typ @ 25°C	Units	Conditions
I_{CC1} [4,5]	Standby Current	3.3V		3		3	1	mA	HALT Mode V_{IN} = OV, V_{CC} @ 8 MHz
[4,5]		5.0V		5		5	2.4	mA	HALT Mode V_{IN} = OV, V_{CC} @ 8 MHz
[4,5]		3.3V		4		4	1.5	mA	HALT Mode V_{IN} = OV, V_{CC} @ 12 MHz
[4,5]		5.0V		6		6	3.2	mA	HALT Mode V_{IN} = OV, V_{CC} @ 12 MHz
[4,5]		3.3V		2		2	0.8	mA	Clock Divide by 16 @ 8 MHz
[4,5]		5.0V		4		4	1.8	mA	Clock Divide by 16 @ 8 MHz
[4,5]		3.3V		3		3	1.2	mA	Clock Divide by 16 @ 12 MHz
[4,5]		5.0V		5		5	2.5	mA	Clock Divide by 16 @ 12 MHz
I_{CC2}	Standby Current	3.3V		8		15	1	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is not Running [6]
		5.0V		10		20	2	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is not Running [6]
		3.3V		500		600	310	µA	STOP Mode V_{IN} = OV, V_{CC} WDT is Running [6]
		5.0V		800		1000	600	µA	S T O P Mode V_{IN} = OV, V_{CC} WDT is

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	T_A = -40°C to +105°C 8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TdA(AS)	Address Valid to	3.3	55		35		55		35		ns	[2]
		/AS Rising Delay	5.0	55		35		55		35		ns	
2	TdAS(A)	/AS Rising to Address	3.3	70		45		70		45		ns	[2]
		Float Delay	5.0	70		45		70		45		ns	
3	TdAS(DR)	/AS Rising to Read	3.3		400		250		400		250	ns	[1,2]
		Data Required Valid	5.0		400		250		400		250	ns	
4	TwAS	/AS Low Width	3.3	80		55		80		55		ns	[2]
			5.0	80		55		80		55		ns	
5	Td	Address Float to	3.3	0		0		0		0		ns	
		/DS Falling	5.0	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	3.3	300		200		300		200		ns	[1,2]
			5.0	300		200		300		200		ns	
7	TwDSW	/DS (Write) Low Width	3.3	165		110		165		110		ns	[1,2]
			5.0	165		110		165		110		ns	
8	TdDSR(DR)	/DS Falling to Read	3.3		260		150		260		150	ns	[1,2]
		Data Required Valid	5.0		260		160		260		160	ns	
9	ThDR(DS)	Read Data to	3.3	0		0		0		0		ns	[2]
		/DS Rising Hold Time	5.0	0		0		0		0		ns	
10	TdDS(A)	/DS Rising to Address	3.3	85		45		85		45		ns	[2]
		Active Delay	5.0	95		55		95		55		ns	
11	TdDS(AS)	/DS Rising to /AS	3.3	60		30		60		30		ns	[2]
		Falling Delay	5.0	70		45		70		45		ns	
12	TdR/W(AS)	R//W Valid to /AS	3.3	70		45		70		45		ns	[2]
		Rising Delay	5.0	70		45		70		45		ns	
13	TdDS(R/W)	/DS Rising to	3.3	70		45		70		45		ns	[2]
		R//W Not Valid	5.0	70		45		70		45		ns	
14	TdDW(DSW)	Write Data Valid to /DS	3.3	80		55		80		55		ns	[2]
		Falling (Write) Delay	5.0	80		55		80		55		ns	
15	TdDS(DW)	/DS Rising to Write	3.3	70		45		70		45		ns	[2]
		Data Not Valid Delay	5.0	80		55		80		55		ns	
16	TdA(DR)	Address Valid to Read	3.3		475		310		475		310	ns	[1,2]
		Data Required Valid	5.0		475		310		475		310	ns	
17	TdAS(DS)	/AS Rising to	3.3	100		65		100		65		ns	[2]
		/DS Falling Delay	5.0	100		65		100		65		ns	
18	TdDI(DS)	Data Input Setup to	0.0	115		115		115		115		ns	[1,2]
		/DS Rising	5.0	75		75		75		75		ns	
19	TdDM(AS)	/DM Valid to /AS	3.3	55		35		55		35		ns	[2]
		Falling Delay	5.0	55		35		55		35		ns	

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

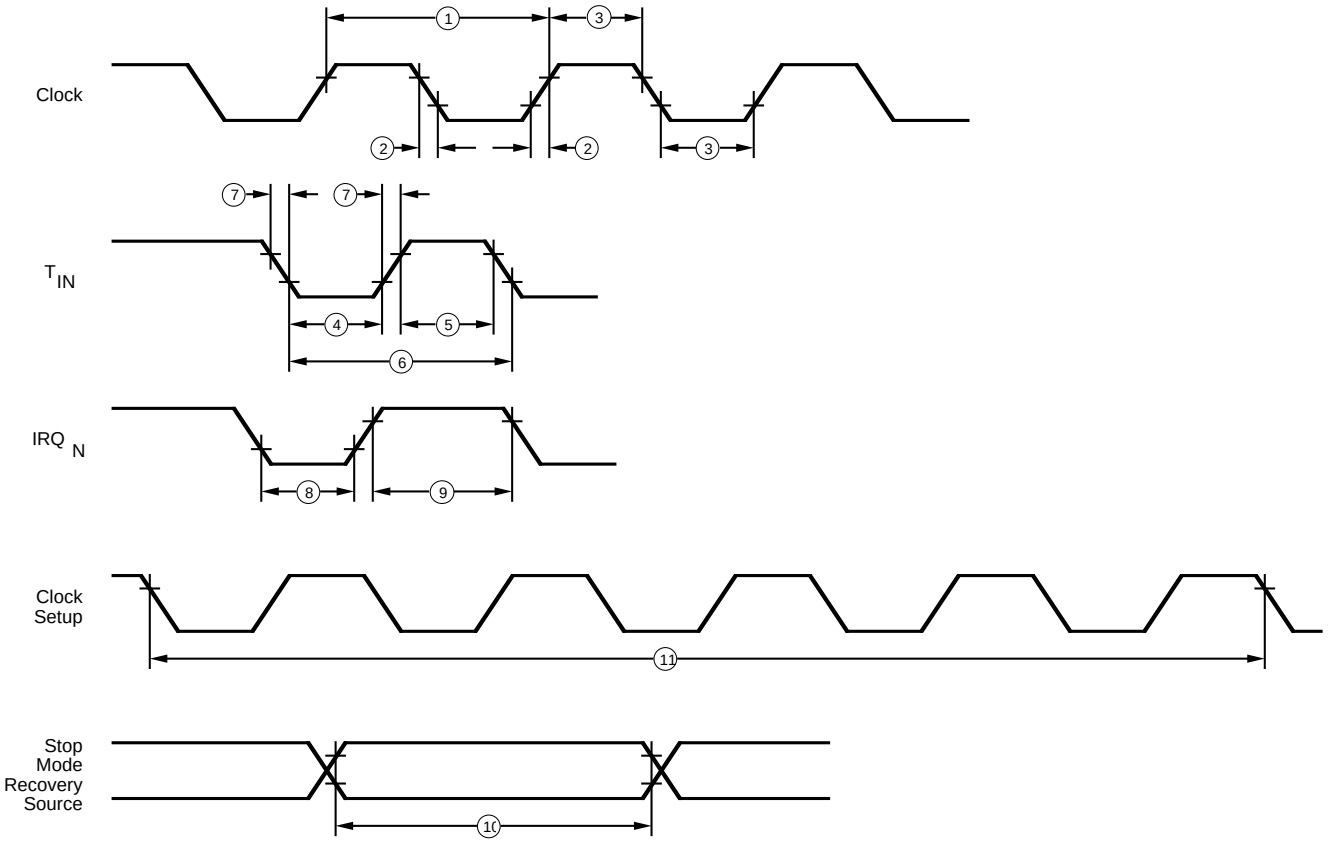
[3] 5.0V ±0.5V, 3.3V ±0.3V.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC CHARACTERISTICS

Additional Timing Table

No	Symbol	Parameter	V_{CC}	T_A = 0°C to 70°C				T_A = -40°C to 105°C				Units	Notes
			Note[6]	8 MHz		12 MHz		8 MHz		12 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.3V	125	100000	83	100000	125	100000	83	100000	ns	[1]
			5.0V	125	100000	83	100000	125	100000	83	100000	ns	[1]
2	TrC,TfC	Clock Input Rise	3.3V		25		15		25		15	ns	[1]
		and Fall Times	5.0V		25		15		25		15	ns	[1]
3	TwC	Input Clock Width	3.3V	37		26		37		26		ns	[1]
			5.0V	37		26		37		26		ns	[1]
4	TwTinL	Timer Input	3.3V	100		100		100		100		ns	[1]
		Low Width	5.0V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input	3.3V	3TpC		3TpC		3TpC		3TpC			[1]
		High Width	5.0V	3TpC		3TpC		3TpC		3TpC			[1]
6	TpTin	Timer Input Period	3.3V	8TpC		8TpC		8TpC		8TpC			[1]
			5.0V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin,TfTin	Timer Input Rise	3.3V		100		100		100		100	ns	[1]
		and Fall Timers	5.0V		100		100		100		100	ns	[1]
8A	TwIL	Interrupt Request	3.3V	100		100		100		100		ns	[1,2]
		Low Time	5.0V	70		70		70		70		ns	[1,2]
8B	TwIL	Int. Request	3.3V	3TpC		3TpC		3TpC		3TpC			[1,3]
		Low Time	5.0V	3TpC		3TpC		3TpC		3TpC			[1,3]
9	TwIH	Interrupt Request	3.3V	3TpC		3TpC		3TpC		3TpC			[1,2]
		Input High Time	5.0V	3TpC		3TpC		3TpC		3TpC			[1,2]
10	Twsm	STOP Mode	3.3V	12		12		12		12		ns	
		Recovery Width Spec	5.0V	12		12		12		12		ns	
			3.3V	5TpC									[7]
			5.0V	5TpC									[8]

AC CHARACTERISTICS

Additional Timing Table (Continued)

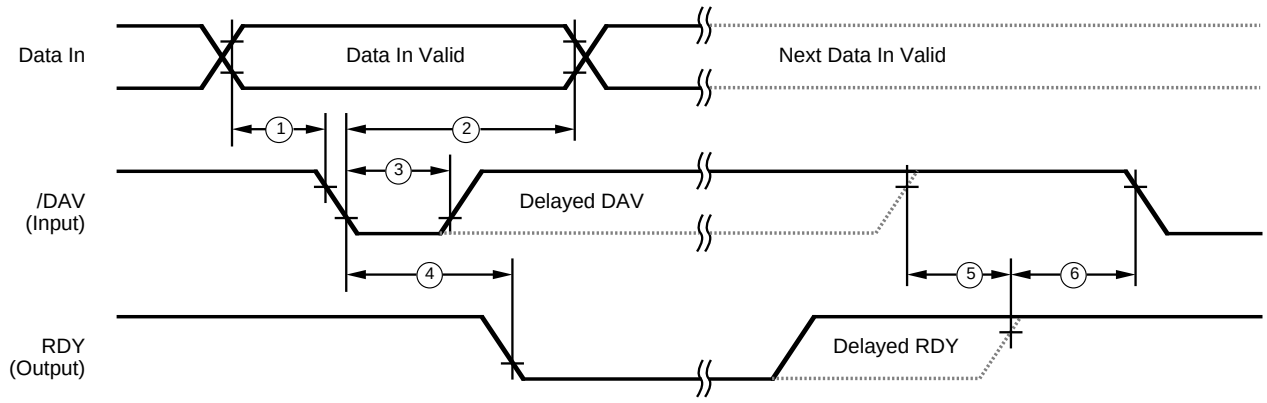
No	Symbol	Parameter	V_{CC} Note[6]	T_A = 0°C to 70°C 8 MHz Min	Max	12 MHz Min	Max	T_A = -40°C to 105°C 8 MHz Min	Max	12 MHz Min	Max	Units	Notes
11	Tost	Oscillator	3.3V		5TpC		5TpC		5TpC		5TpC		[4]
		Startup Time	5.0V		5TpC		5TpC		5TpC		5TpC		[4]
12	Twdt	Watchdog Timer	3.3V	10		10		10		10		ms	D0 = 0 [5]
		Delay Time	5.0V	5		5		5		5		ms	D1 = 0 [5]
			3.3V	30		30		30		30		ms	D0 = 1 [5]
			5.0V	15		15		15		15		ms	D1 = 0 [5]
			3.3V	50		50		50		50		ms	D0 = 0 [5]
			5.0V	25		25		25		25		ms	D1 = 1 [5]
			3.3V	200		200		200		200		ms	D0 = 1 [5]
			5.0V	100		100		100		100		ms	D1 = 1 [5]

Notes:

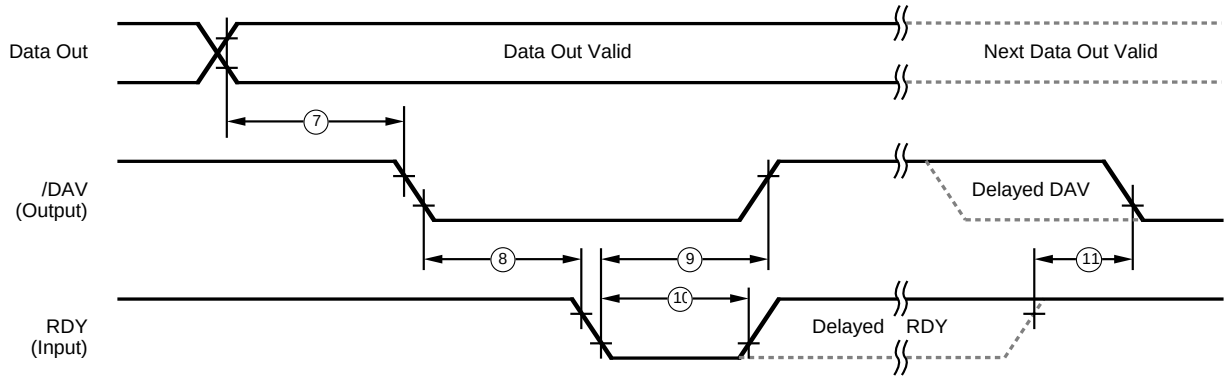
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 0
[5] Reg. WDTMR
[6] 5.0V ±0.5V, 3.3V ±0.3V
[7] Reg. SMR - D5=0
[8] Reg. SMR - D5=1

AC CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note[1]	T_A = 0°C To 70° C				T_A = -40° C To 105° C				Data Direction
				8 MHz		12 MHz		8 MHz		12 MHz		
				Min	Max	Min	Max	Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	3.3V	0		0		0		0		IN
			5.0V	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	3.3V	160		160		160		160		IN
			5.0V	115		115		115		115		IN
3	TwDAV	Data Available Width	3.3V	155		155		155		155		IN
			5.0V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	3.3V		160		160		160		160	IN
		Falling Delay	5.0V		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	3.3V		120		120		120		120	IN
		Falling Delay	5.0V		80		80		80		80	IN
6	TdDO(DAV)	RDY Rising to DAV	3.3V	0		0		0		0		IN
		Falling Delay	5.0V	0		0		0		0		IN
7	TcLDAV0(RDY)	Data Out to DAV	3.3V	63		42		63		42		OUT
		Falling Delay	5.0V	63		42		63		42		OUT
8	TcLDAV0(RDY)	DAV Falling to RDY	3.3V	0		0		0		0		OUT
		Falling Delay	5.0V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	3.3V		160		160		160		160	OUT
		Rising Delay	5.0V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.3V	110		110		110		110		OUT
			5.0V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	3.3V		110		110		110		110	OUT
		Falling Delay	5.0V		80		80		80		80	OUT

Note:
[1] 5.0 V ±0.5V, 3.3V ±0.3V

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