Z86C96
CMOS Z8® MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C96 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C96 is a member of the Z8 single-chip microcontroller family with 256 bytes of general-purpose RAM.

The MCU is housed in 64-pin DIP and 68-pin Leaded Chip-Carrier packages and is manufactured in CMOS technology.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C96 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced consumer applications.

The device applications demand powerful I/O capabilities. The Z86C96 fulfills this with 52 pins dedicated to input and output. These lines are grouped into six 8-bit ports and one 4-bit port. The ports are configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: program memory, data memory and 236 general-purpose registers.

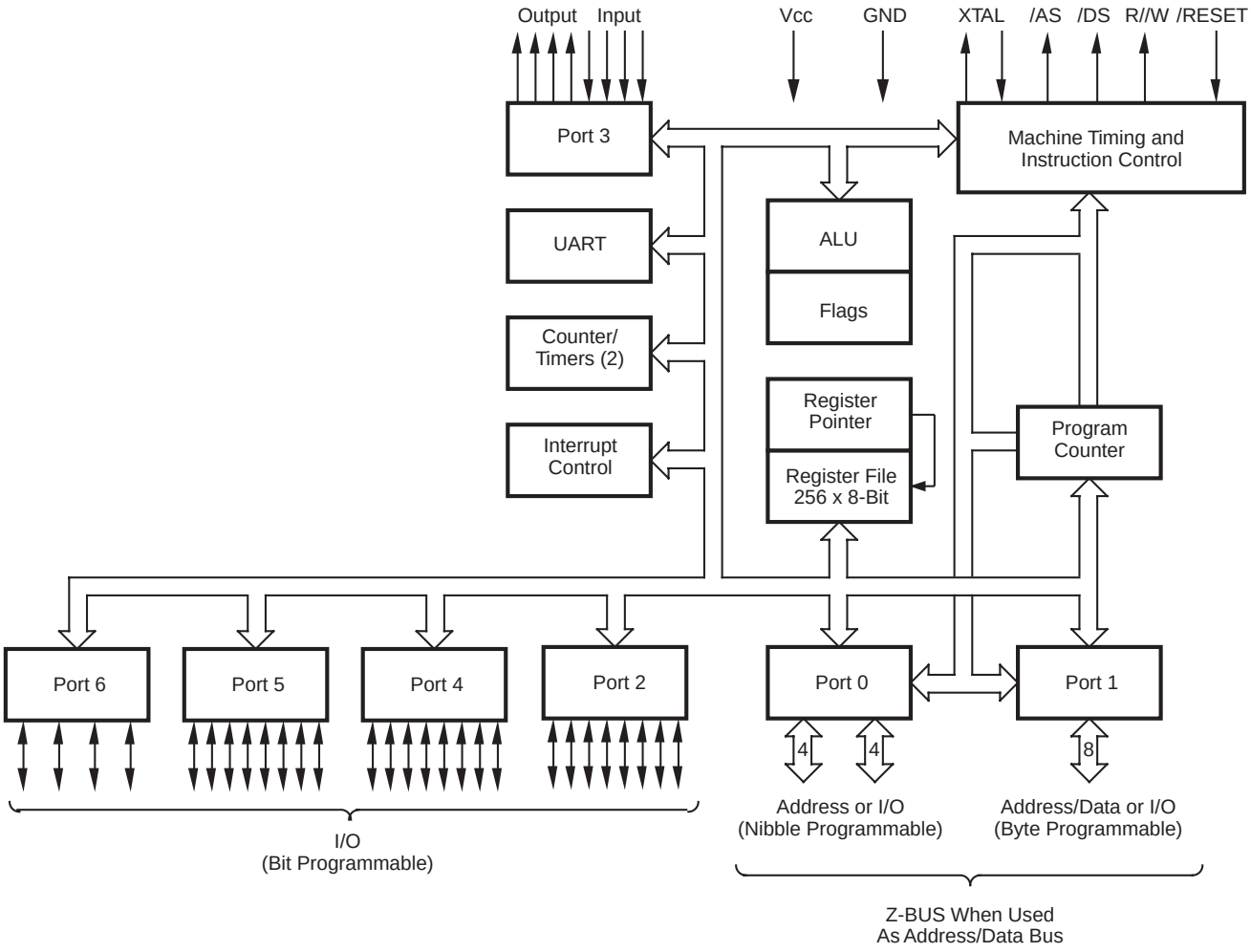
To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C96 offers two on-chip Counter/Timers with a large number of user selectable modes, and a Asynchronous Receiver/Transmitter (UART - see block diagram).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

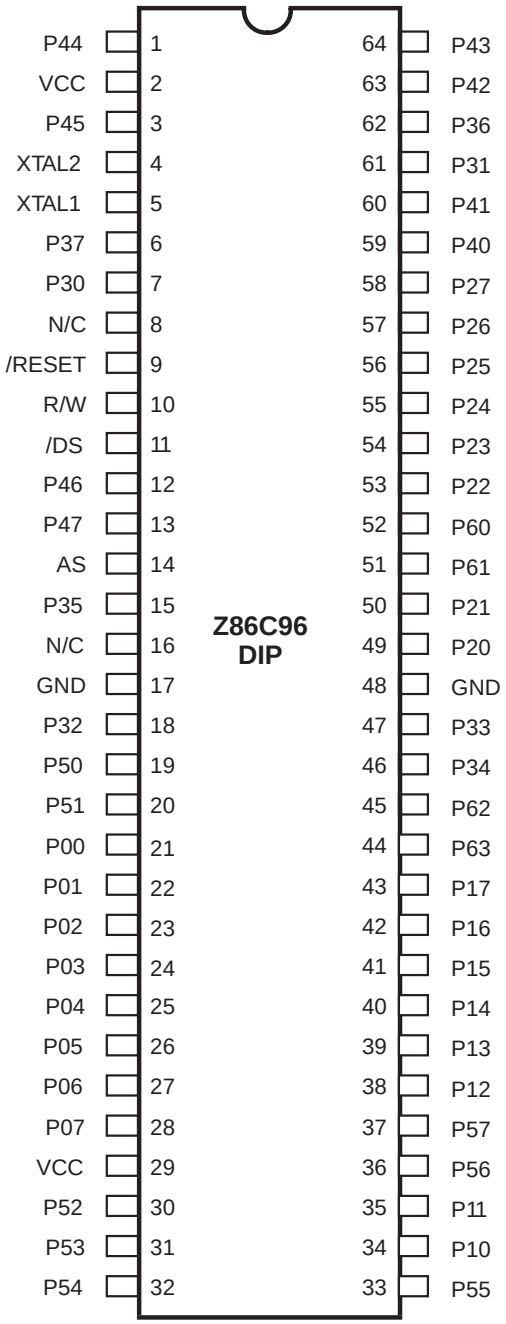
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



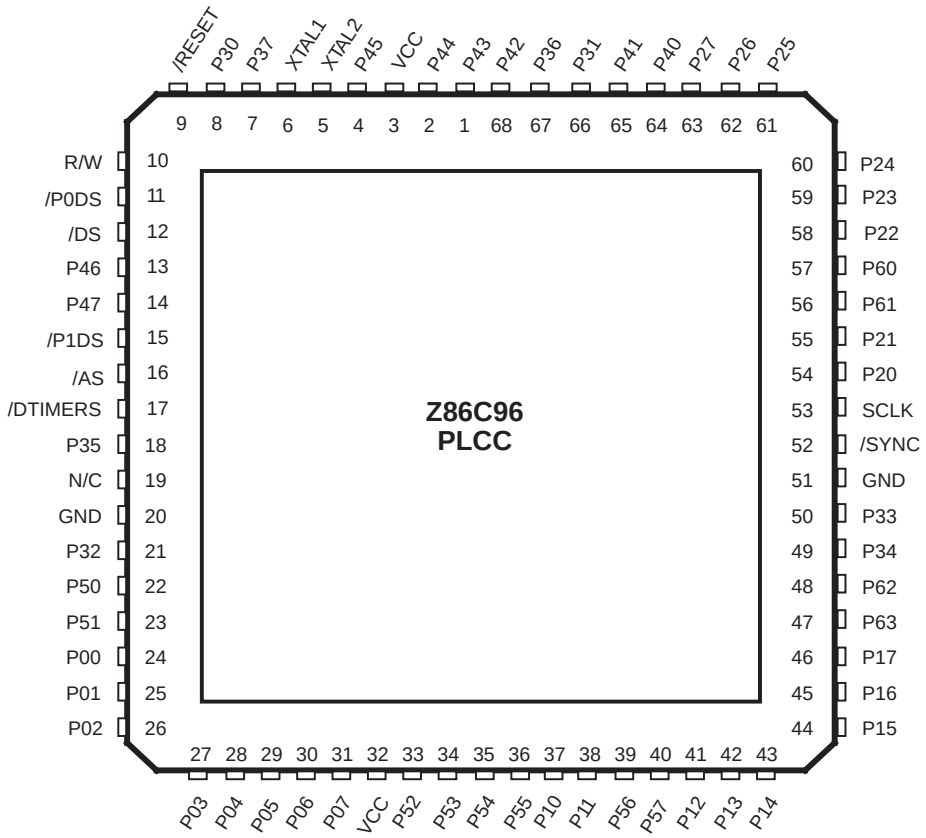
Functional Block Diagram

PIN DESCRIPTION



64-Pin Dual In-Line Plastic Pin Assignments

PIN DESCRIPTION (Continued)



68-Pin Plastic Leaded Chip Carrier Pin Assignments

ABSOLUTE MAXIMUM RATINGS

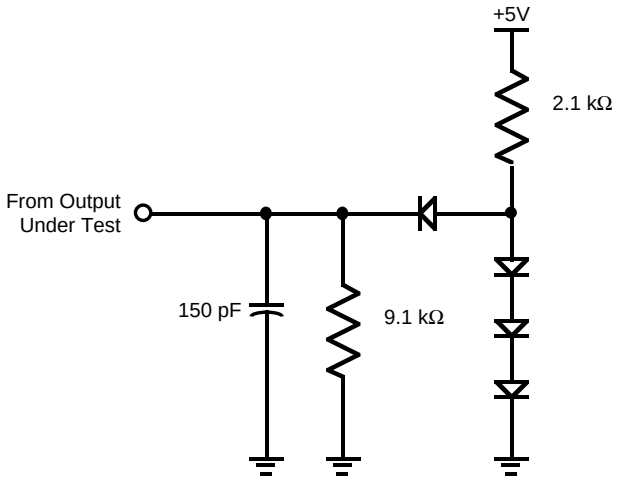
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Test Load Diagram).



Test Load Diagram

PLEASE NOTE

This device will not operate in extended Timing mode. Set Register 248 (F8H), D5 = 0.

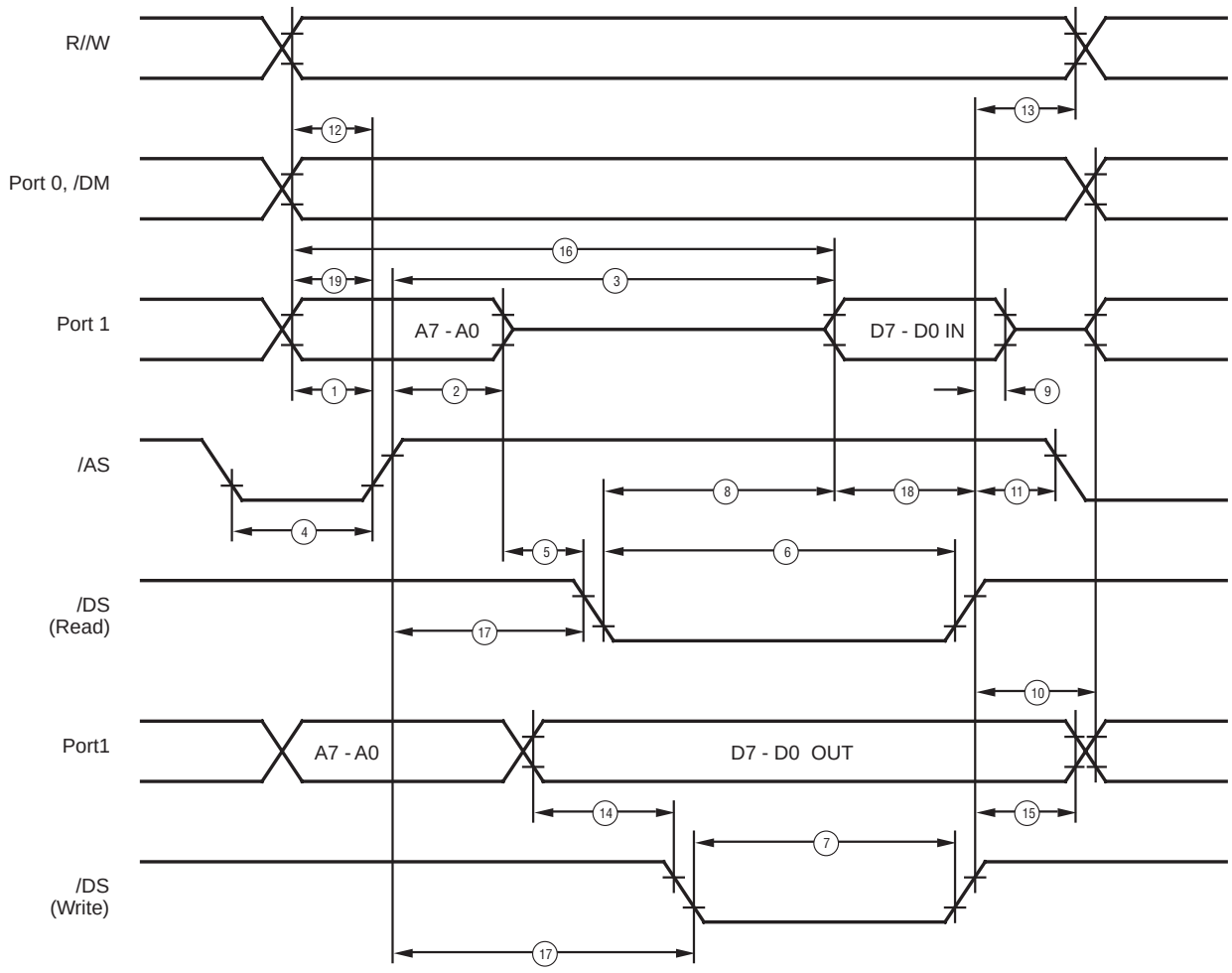
DC CHARACTERISTICS

Sym	Parameter VCC = 4.5 V to 5.5 V	T_A = 0°C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+ 0.3	3.8	V_{CC}+ 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}+ 0.3	2.0	V_{CC}+ 0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
V_{OH}	Output High Voltge	2.4		2.4			V	I_{OH} = -2.0 mA
V_{OH}	Output High Voltge	V_{CC}–100mV		V_{CC}–100mV			V	I_{OH} = -100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+ 0.3	3.8	V_{CC}+ 0.3		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8	–0.3	0.8		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0 V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	V_{RL} = 0 V
I_{CC}	Supply Current		35		35	24	mA	[1] @ 16 MHz
I_{CC1}	Standby Current		6.5		6.5	4	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC}@12 MHz
			7.0		7.0	4.5	mA	[1] HALT Mode V_{IN} = 0 V,V_{CC}@ 16 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1] STOP Mode V_{IN} = 0 V,V_{CC}

Notes:
[1] All inputs driven to either 0 V or V_{CC}, outputs floating.

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Table

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	T_A = –40°C to +105°C 16 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	25		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	35		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		180		180	ns	[1,2,3]
4	TwAS	/AS Low Width	40		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width	135		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	80		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		75		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	50		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	35		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	20		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	35		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	25		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		230		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay		45		45	ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise		60		60	ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Rise Delay		30		30	ns	[2,3]

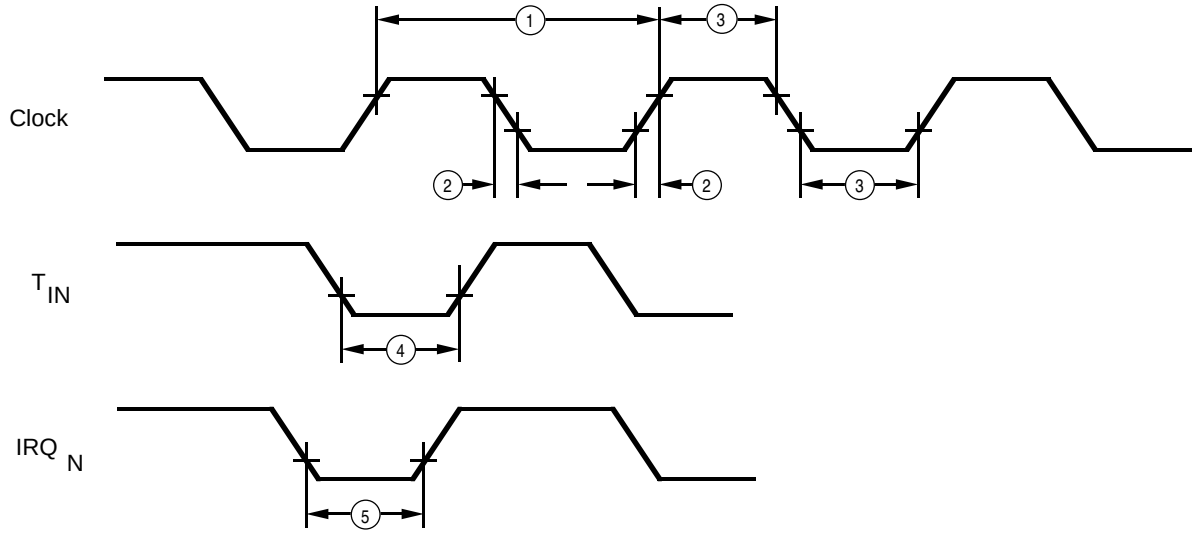
Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See Clock Dependent Formulas table.

Standard Test Load
All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TsDI(DS)	0.8 TpC – 10
19	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS
Additional Timing Diagram



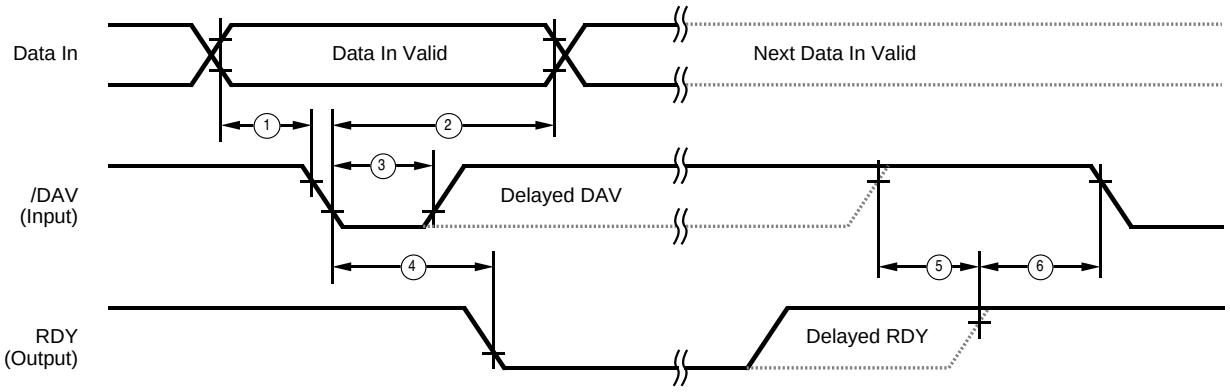
Additional Timing

AC CHARACTERISTICS
Additional Timing Table

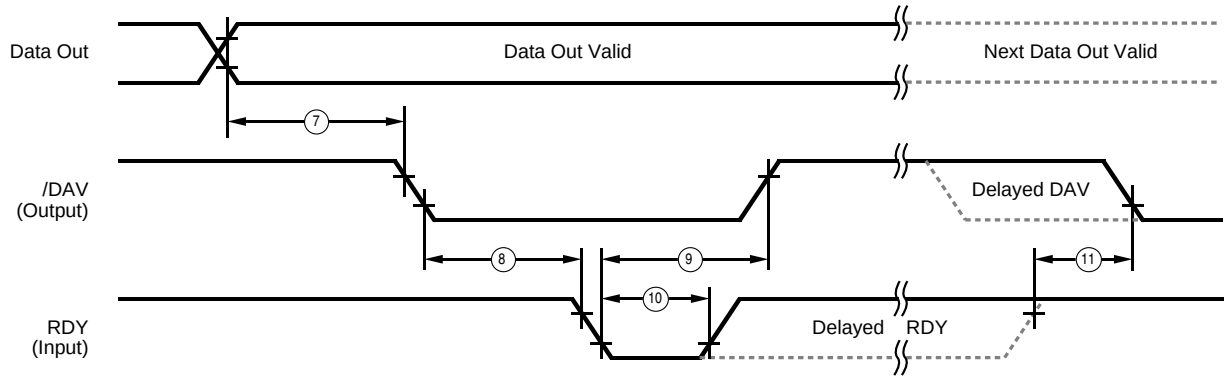
No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	T_A = –40°C to +105°C 16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	62.5	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10		10	ns	[1]
3	TwC	Input Clock Width	25		25		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	3TpC		3TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC			[2,3]

Notes:
[1] Clock timing references use 3.8 V for a logic 1 and 0.8 V for a logic 0.
[2] Timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	T_A = 0°C to +70°C 16 MHz Max	T_A = –40°C to +105°C 16 MHz Min	T_A = –40°C to +105°C 16 MHz Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115	OUT

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specifcation requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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